

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
6	0001395489	ENGINEERING RELEASED	2012-03-13

SCHEM, MLB, J30

03/12/12

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64	PBUS Supply & Battery Charger	JACK_330	09/27/2011
65	System Agent Supply	JACK_330	09/28/2011
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67	1.5V DDR3 Supply	JACK_330	07/28/2011
68	CPU IMVP7 & AXG VCore Regulator	JACK_330	08/03/2011
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Schematic / PCB #'s

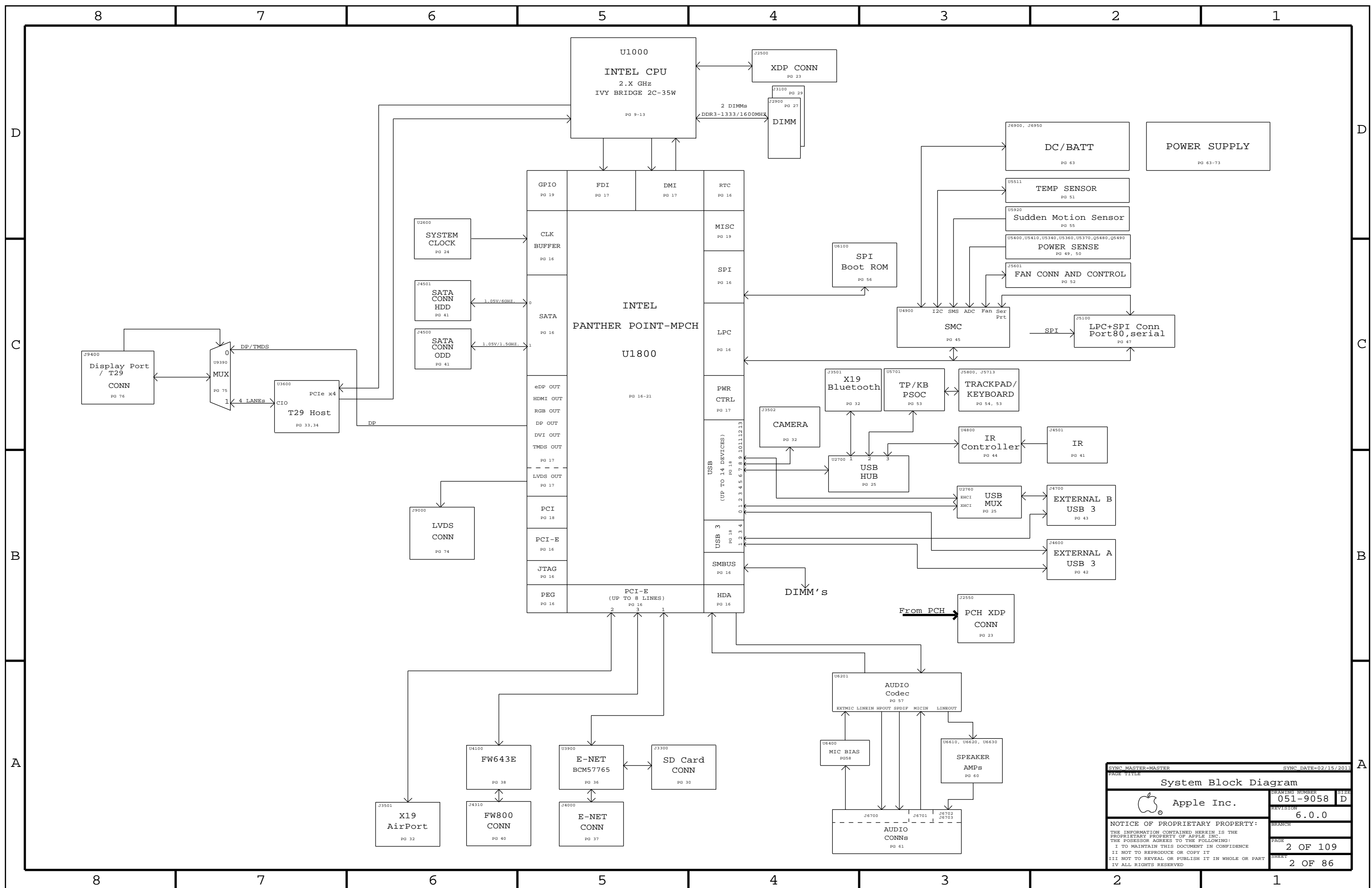
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820-3115	1	PCBF,MLB,J30	PCB	CRITICAL	

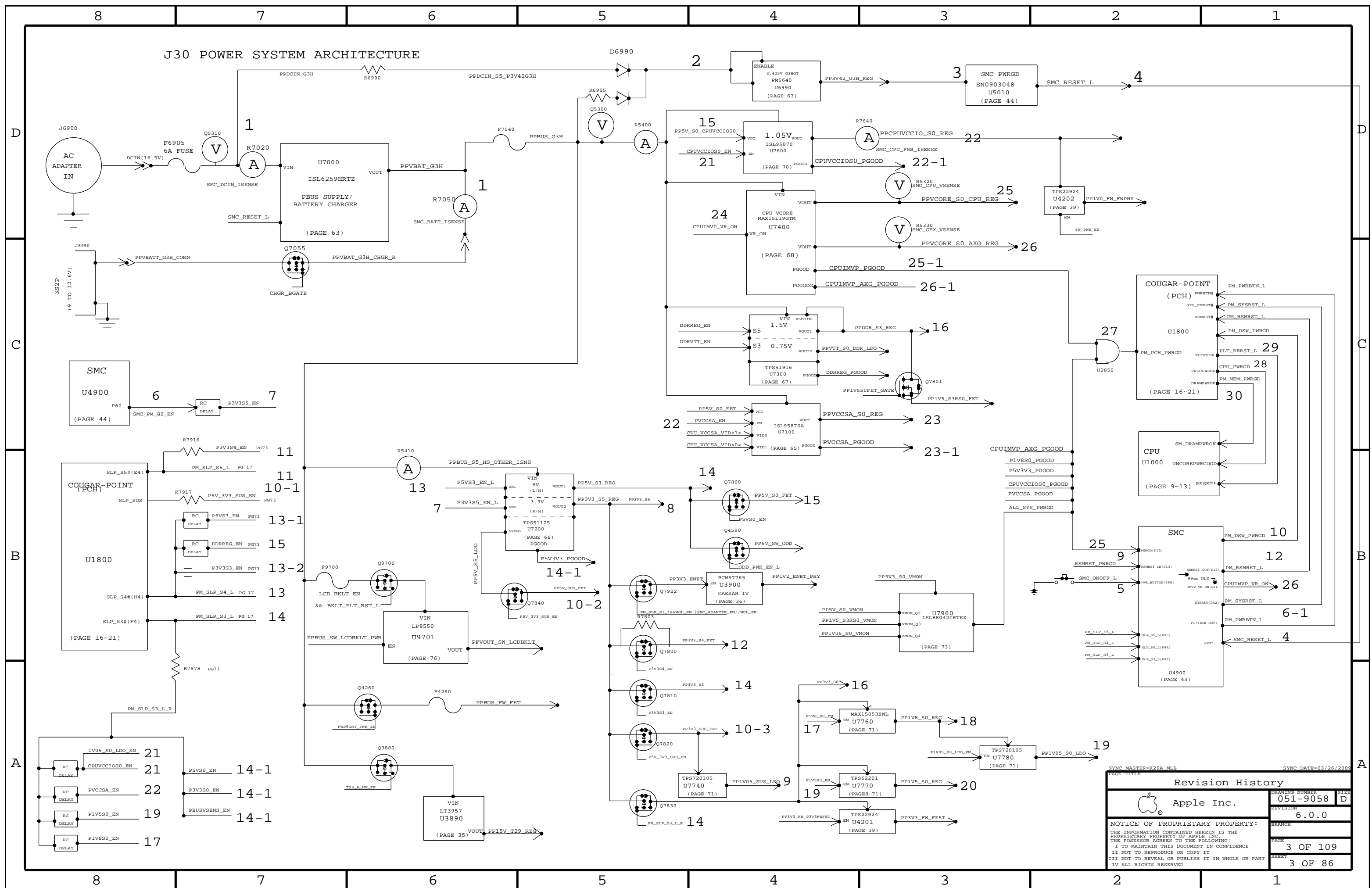
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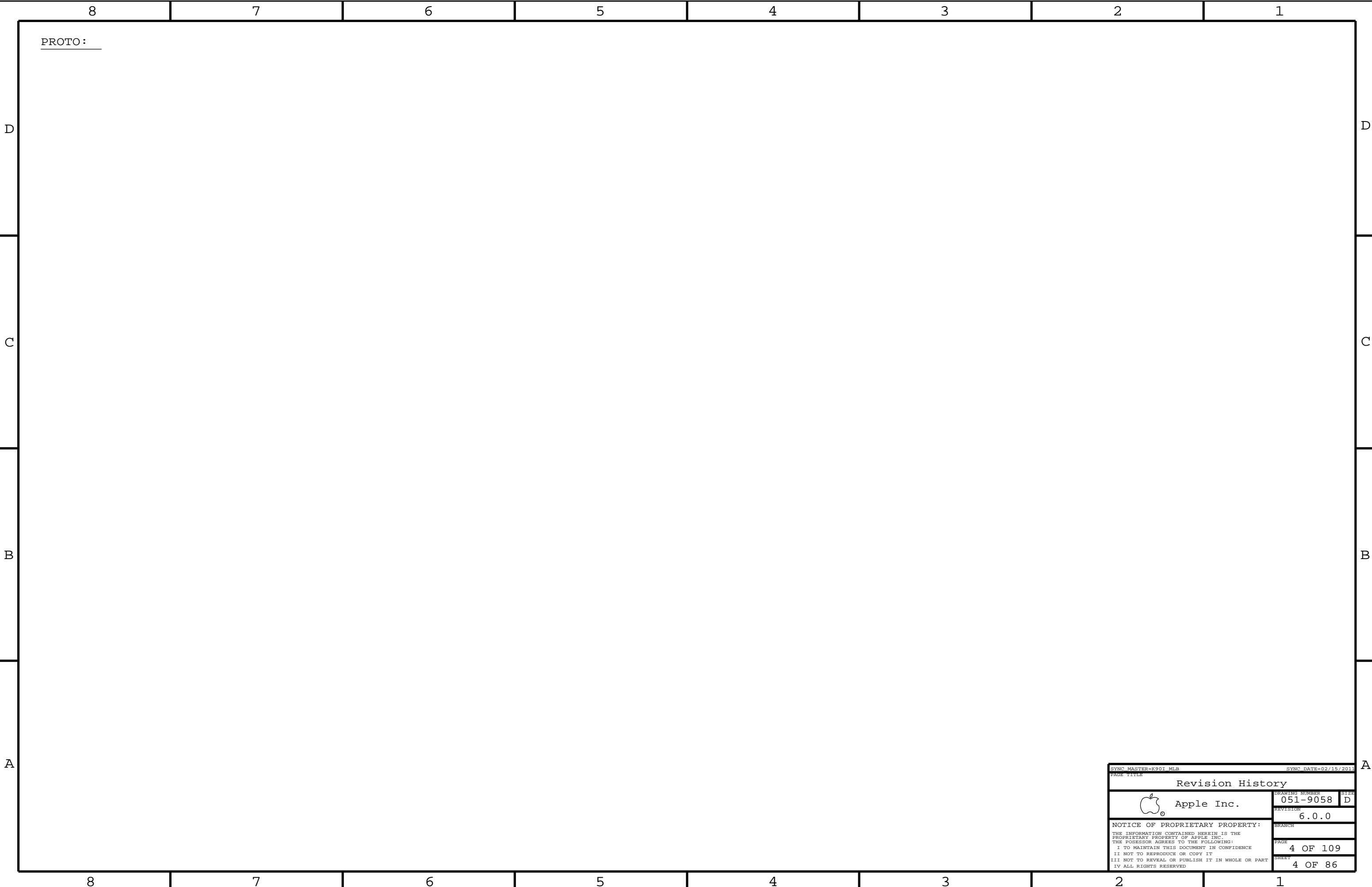
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PROTO:

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2011

Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
607-8895	CMN PTS,PCBA,MLB,J30	J30_COMMON,FET_PAIR
085-3092	J30 MLB DEVELOPMENT BOM	J30_LEVEL:KNG
607-8721	POWER FETS PAIR,FAIRCHILD,DDR,J30	DDR_POWER_FET:PAIR
607-8722	POWER FETS PAIR,FAIRCHILD,5V_S3,J30	5V_S3_POWER_FET:PAIR
607-8723	POWER FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CHARGER_POWER_FET:PAIR
607-9309	POWER FETS PAIR,RENESAS,DDR,J30	DDR_POWER_FET:REN
607-9310	POWER FETS PAIR,RENESAS,5V_S3,J30	5V_S3_POWER_FET:REN
607-9311	POWER FETS PAIR,RENESAS,PBUS_CHARGER,J30	CHARGER_POWER_FET:REN
639-3752	PCBA,MLB,MOL,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:MOLEX,EEEE_F1YK
639-3756	PCBA,MLB,HYB,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:HYBRID,EEEE_F1YH
639-3753	PCBA,MLB,FOX,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:FOXCONN,EEEE_F1YL
639-3755	PCBA,MLB,HYB,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:HYBRID,EEEE_F1YJ
639-3751	PCBA,MLB,MOL,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:MOLEX,EEEE_F1YM
639-3754	PCBA,MLB,FOX,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:FOXCONN,EEEE_F1YG

J30 BOM GROUPS

BOM GROUP	BOM OPTIONS
J30_COMMON	ALTERNATE,COMMON,J30_COMMON1,J30_COMMON2,J30_DEBUG:ENG,J30_PROGPARTS,T29BST:Y,TBTHV:P15V
J30_COMMON1	BATT_3S,CPUMEM_S0,USBHUB2513B,HUB_3NONREM,T29:YES,SDRV_PD,SDRV12C:MCU,AXG_PHASE1,BTQWR:S4,UV_GLUE_J30
J30_COMMON2	MIKEY,TPAD:E2,RAMCFG_SLOT
J30_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
J30_DEVEL:ENG	BKLT:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCLPLUS_CONN:YES,LOADISNS:YES,SDRVREF_DAC,S0FOGOOD_ISL
J30_DEVEL:PVT	LPCLPLUS_CONN:YES,XDP_CONN
J30_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,LPCLPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO_DAC
J30_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCLPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2514B
J30_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCLPLUS_R:YES,LOADISNS:NO,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2513B

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4113	1	IC, IVB, 2C, 35W, 1023MSA	U1000	CRITICAL	CPU_IVB_2C
337S4264	1	IVB, S ROND, PRQ, L1, 2, 5, 35W, 2+2, 1, 1, 3M, BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4265	1	IVB, S ROND, PRQ, L1, 2, 9, 35W, 2+2, 1, 25, 4M, BGA	U1000	CRITICAL	CPU_2_9GHZ
337S4269	1	PANTHERPOINT, C1, BLJRC, PRQ, BD82HM77	U1800	CRITICAL	
343S0534	1	IC, BCM57765B0, ENET&D, 8X8	U3900	CRITICAL	
338S0753	1	IC, FW418E, 1394B, PCI/SMC, 1.0M, PCI-E, 12	U4100	CRITICAL	
338S1072	1	IC, T29, PRQ, S, LJ3Y, FCBGA, 15x15MM, C1	U3600	CRITICAL	T29: YES
353S3055	1	IC, 0133VD0212, X2, DISPLAYPORT 2:1, MIX, QFN	U9390	CRITICAL	
946-3827	1	J30 MIA EYMAX ADDRESSIVE 29993-BC 0.480	UV_GLUE_J30	CRITICAL	UV_GLUE_J30
516S0806	1	CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA, FOXCONN	J3100	CRITICAL	SODIMM: FOXCONN
516-0246	1	CONN, 204P, SODIMM, DDR3, P=0.6MM, FOXCONN	J2900	CRITICAL	SODIMM: FOXCONN
516S0805	1	CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA, MOLEX	J3100	CRITICAL	SODIMM: MOLEX
516-0245	1	CONN, 204P, SODIMM, DDR3, P=0.6MM, MOLEX	J2900	CRITICAL	SODIMM: MOLEX
516S0805	1	CONN, 204P, SODIMM, SOCKET, DDR3, RAM, BGA, MOLEX	J3100	CRITICAL	SODIMM: HYBRID
516-0246	1	CONN, 204P, SODIMM, DDR3, P=0.6MM, FOXCONN	J2900	CRITICAL	SODIMM: HYBRID

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYG]	CRITICAL	EEEE_FLYG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYH]	CRITICAL	EEEE_FLYH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYJ]	CRITICAL	EEEE_FLYJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYK]	CRITICAL	EEEE_FLYK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYL]	CRITICAL	EEEE_FLYL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:FLYM]	CRITICAL	EEEE_FLYM

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0862	1	IC,FLASH,SERIAL,SP1,1MBIT,V27,REV F	U3990	CRITICAL	ENET_BLANK
341S3096	1	IC ENET,11MBITFLAN,CIV REV01,K9x	U3990	CRITICAL	ENET_PROG
335S0550	1	IC,EEPROM,SERIAL,SP1,4Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341S3430	1	IC,T29 EEPROM,LR,J30/J31	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S3365	1	IC,PROGRMD,T29,PORT MCU,K901A,K91A,K92A	U9330	CRITICAL	T29MCU:PROG
336S1098	1	IC,SMC12-A3,40MHZ/50MDIPS MCU,9x9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3300	1	IC,SMC,EXTERNAL,FSB,A3,J30	U4900	CRITICAL	SMC_PROG
335S0807	1	IC,SP1 SML 50MHZ FLASH,64MBT,820P,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK
335S0812	1	64 MBIT SP1 SRL DUAL I/O FLASH,801CS	U6100	CRITICAL	BOOTROM_BLANK
341S3558	1	IC,EFI,V00C7,J30/J31	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	1R,ENCORE II, CV7C63903-LQMC	U4800	CRITICAL	
341S3522	1	IC,PSOC,TP/KB,J30/J31	U5701	CRITICAL	TPAD_PROG


Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
11880603	11880602		ALL	Murata alt to Samsung
15780058	15780084		ALL	Infra alt to VM Negative
12803303	12803353		ALL	Paranchoil alt to Samsung
11880676	11880691		ALL	Murata alt to Samsung
15200778	15200693		ALL	Cyber alt to Vishay
37608955	37601032		ALL	Siobas alt to Toshiba
37608977	37608959		ALL	Siobas alt to Toshiba
37608972	37601017		ALL	Siobas alt to Toshiba
37608937	37608945		ALL	Fairchild alt to Renesas
37608777	37608761		ALL	ADM alt to Siliconix
37608957	37608958		ALL	Fairchild alt to Fairchild
37608953	37608958		ALL	Fairchild alt to Renesas
37780107	37780126		ALL	Omron alt to Omron
37180709	37180652		ALL	ROP alt to Infineon
514-0788	514-0671		ALL	Analogic Litecam alt to Anson
607-9310	607-8722		ALL	Renesas alternate to fairchild
607-9311	607-8723		ALL	Renesas alternate to fairchild

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15201499	15200864		ALL	Culivcraft alt to Murata
15201493	15201300		ALL	Culivcraft alt to Murata
13800692	13800648		ALL	Samsung/Murata alt to Taiyo
13800684	13800640		ALL	Murata alt to Taiyo
15201512	15201295		ALL	Cytron alt to MDC
15201019	15201271		ALL	Cytron alt to WDM
37601023	37600960		ALL	Siliconix alt to Renesas
35303312	35303055		ALL	NSP alt to Pericom
35303238	35301428		ALL	Intersil alt to TI
35303519	35302179		ALL	Intersil alt to TI
15800578	15800367		ALL	Taiyo alt to Murata
13800681	13800638		ALL	Taiyo alt to Samsung
13800671	13800673		ALL	Taiyo alt to Murata
37600903	37600786		ALL	Fairchild alt to Vishay
37700124	37700057		ALL	Amtech alt to TDK
34103492	34103096		ALL	Murata alt to Mamei (RUBY ROW)
37601053	37600604		ALL	Siemens alt to Fairchild
37601076	37600634		ALL	Siemens alt to mamei

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3092	1	J30 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8895	1	CMN PTS,PCBA,MLB,J30	CMNPTS	CRITICAL	J30_CMNPTS
607-8721	1	POWER_FETS PAIR,FAIRCHILD,DDR,J30	CSET1	CRITICAL	FET_PAIR
607-8732	1	POWER_FETS PAIR, FAIRCHILD, 5V,S3,J30	CSET2	CRITICAL	FET_PAIR
607-8723	1	POWER_FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CSET3	CRITICAL	FET_PAIR

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
BOM Configuration			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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Functional Test Points

D

Fan Connectors

613	TRUE	PP5V_S0	6	7
615	TRUE	FAN_RT_PWM	52	
616	TRUE	FAN_RT_TACH	52	

(NEED TO ADD 1 GND TP)

MIC_FUNC_TEST

650	TRUE	BI_MIC_LO	61	62
650	TRUE	BI_MIC_HI	61	62
650	TRUE	BI_MIC_SHIELD	61	62

(NEED TO ADD 1 GND TP)

SPEAKER_FUNC_TEST

660	TRUE	SPKRAMP_L_N_OUT	60	61	85
660	TRUE	SPKRAMP_L_P_OUT	60	61	85
660	TRUE	SPKRAMP_R_N_OUT	60	61	85
660	TRUE	SPKRAMP_R_P_OUT	60	61	85
660	TRUE	SPKRAMP_SUB_N_OUT	60	61	85
660	TRUE	SPKRAMP_SUB_P_OUT	60	61	85

X19_CONN

660	TRUE	PP3V3_WLAN	(NEED 3 TP)	6	32	46
660	TRUE	PCIE AP D2R PI P		32	81	
660	TRUE	PCIE AP D2R PI N		32	81	
660	TRUE	PCIE AP R2D P		32	81	
660	TRUE	PCIE AP R2D N		32	81	
660	TRUE	PCIE CLK100M AP CONN P		32	85	
660	TRUE	PCIE CLK100M AP CONN N		32	85	
660	TRUE	PP3V3_S3RS4_BT_F		32		
660	TRUE	PCIE_WAKE_L		17	24	32
660	TRUE	USB_BT_CONNN_P		32	80	
660	TRUE	USB_BT_CONNN_N		32	80	
660	TRUE	AP_CLKREQ_Q_L		32		
660	TRUE	AP_RESET_CONNN_L		32		
660	TRUE	AP_TEMP_SMB_SDA_R		32		
660	TRUE	AP_TEMP_SMB_SCL_R		32		
660	TRUE	WIFI_EVENT_L_R		32		
		(NEED 70 AND 5 GND TP)				

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

660	TRUE	PP3V3_S4	6	7
660	TRUE	PP18V5_Z2	6	54
660	TRUE	Z2_CS_L	53	54
660	TRUE	Z2_DEBUG3	53	54
660	TRUE	Z2_MOSI	53	54
660	TRUE	Z2_MISO	53	54
660	TRUE	Z2_SCLK	53	54
660	TRUE	Z2_BOOST_EN	54	
660	TRUE	Z2_HOST_INTN	53	54
660	TRUE	Z2_CLKIN	53	54
660	TRUE	Z2_KEY_ACT_L	53	54
660	TRUE	Z2_RESET	53	54
660	TRUE	PSOC_MISO	53	54
660	TRUE	PSOC_MOSI	53	54
660	TRUE	PSOC_SCLK	53	54
660	TRUE	SMBUS_SMC_2_S3_SCL	6	45 48
660	TRUE	SMBUS_SMC_2_S3_SDA	6	45 48
660	TRUE	PSOC_F_CS_L	53	54
660	TRUE	PICKB_L	53	54
660	TRUE	PP5V_S5_CUMULUS	54	

(NEED TO ADD 2 GND TP)

KEYBOARD_CONN

660	TRUE	PP3V3_S4	6	7
660	TRUE	PP3V42_G3H	6	7
660	TRUE	WS_KBD1	53	
660	TRUE	WS_KBD2	53	
660	TRUE	WS_KBD3	53	
660	TRUE	WS_KBD5	53	
660	TRUE	WS_KBD6	53	
660	TRUE	WS_KBD7	53	
660	TRUE	WS_KBD8	53	
660	TRUE	WS_KBD9	53	
660	TRUE	WS_KBD10	53	
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660	TRUE	WS_KBD20	53	
660	TRUE	WS_KBD21	53	
660	TRUE	WS_KBD22	53	
660	TRUE	WS_KBD23	53	
660	TRUE	WS_KBD_ONOFF_L	53	
660	TRUE	WS_LEFT_SHIFT_KBD	53	
660	TRUE	WS_LEFT_OPTION_KBD	53	
660	TRUE	WS_CONTROL_KBD	53	

(NEED TO ADD 2 GND TP)

KBD_BACKLIGHT_CONN

660	TRUE	KBDLED_ANODE	54	
660	TRUE	SMC_KBDLED_PRESENT_L	54	

(NEED TO ADD 1 GND TP)

CAMERA/ALS_CONN

PC006	TRUE	PP5V_S3_ALSCAMERA_F	32	
PC006	TRUE	SMBUS_SMC_2_S3_SCL	6	45 48 84
PC006	TRUE	SMBUS_SMC_2_S3_SDA	6	45 48 84
PC007	TRUE	USB_CAMERA_CONN_P	32	80
PC008	TRUE	USB_CAMERA_CONN_N	32	80

(NEED TO ADD 2 GND TP)

(NEED TO ADD 2 GND TP)

BATT_POWER_CONN

630	TRUE	SMC_BIL_BUTTON_L	45	46
632	TRUE	SMC_LID_R		63
638		(NEED TO ADD 2 GND TP)		

(NEED TO ADD 5 GND TP)

BIL_CONN

660	TRUE	PP3V42_G3H	6	7
660	TRUE	SMBUS_SMC_5_G3_SCL	6	45 48
660	TRUE	SMBUS_SMC_5_G3_SDA	6	45 48
660	TRUE	SMC_BIL_BUTTON_L	45	46
660	TRUE	SMC_LID_R	63	

(NEED TO ADD 2 GND TP)

(NEED TO ADD 2 GND TP)

DEBUG_VOLTAGE

660	TRUE	PPVCORE_S0_CPU	7	
660	TRUE	PPVCORE_S0_AXG	7	
660	TRUE	PP1V2_S3_ENET_INTREG	71	
660	TRUE	PP1V05_S0	7	
660	TRUE	PP1V5_S3RS0	7	85
660	TRUE	PP1V8_S0	7	
660	TRUE	PP3V3_S0	7	85
660	TRUE	PP5V_S0	6	7
660	TRUE	PP3V3_S3	7	
660	TRUE	PP5V_S3	7	
660	TRUE	PPVCCSA_S0_CPU	7	
660	TRUE	PP3V3_S5	7	85
660	TRUE	PP3V42_G3H	6	7
660	TRUE	PPBUS_G3H	7	
660	TRUE	PP3V3_ENET	7	
660	TRUE	PP3V3_WLAN	6	32 46
660	TRUE	PP5V_SW_ODD	6	41
660	TRUE	PP5V_S0_HDD_FLT	6	41
660	TRUE	PP18V5_Z2	6	54
660	TRUE	PP3V3_S0_LCD_F	6	74
660	TRUE	PP3V3_LCDVDD_SW_F	6	74
660	TRUE	PP4V5_AUDIO_ANALOG	57	62
660	TRUE	PP1V5_S3	7	
660	TRUE	SMC_PM_G2_EN	45	73
660	TRUE	PM_SLP_S4_L	17	26 32 45 73
660	TRUE	PM_SLP_S3_L	8	17 26 45 73

(NEED TO ADD 6 GND TP)

(NEED TO ADD 6 GND TP)

DC_POWER_CONN

660	TRUE	PP18V5_DCIN_FUSE	63	
660	TRUE	ADAPTER_SENSE	63	

(NEED TO ADD 4 GND TP)

LPC+SPI_DEBUG_CONN

660	TRUE	LPC_AD<0>	16	45	47	81
660	TRUE	LPC_AD<1>	16	45	47	81
660	TRUE	LPC_AD<2>	16	45	47	81
660	TRUE	LPC_AD<3>	16	45	47	81
660	TRUE	LPC_CLK33M LPCPLUS	24	47	81	
660	TRUE	LPC_FRAME_L	16	45	47	81
660	TRUE	LPC_PWRDWN_L	17	45	47	
660	TRUE	LPC_SERIRO	16	45	47	
660	TRUE	LPCPLUS_GPIO	19	47		
660	TRUE	LPCPLUS_RESET_L	24	47		
660	TRUE	PM_CLKRUN_L	17	45	47	
660	TRUE	PP3V42_G3H	6	7		
660	TRUE	PP5V_S0	6	7		
660	TRUE	SMC_RX_L	45	46	47	
660	TRUE	SMC_TCK	45	46	47	
660	TRUE	SMC_TDI	45	46	47	
660	TRUE	SMC_TDO	45	46	47	
660	TRUE	SMC_TMS	45	46	47	
660	TRUE	SMC_TX_L	45	46	47	
660	TRUE	SPI_ALT_CLK	47			
660	TRUE	SPI_ALT_CS_L	47			
660	TRUE	SPI_ALT_MISO	47			
660	TRUE	SPI_ALT_MOSI	47			
660	TRUE	SPIROM_USE_MLB	19	47	56	

(NEED TO ADD 2 GND TP)

(NEED TO ADD 2 GND TP)

NC_NO_TESTS

17	TP_CRT_IG_BLUE	==	TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	==	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	==	MAKE_BASE=TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	==	TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	==	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	==	TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	==	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
17	TP_LVDS_IG_CTRL_CLK	==	TRUE	NC_LVDS_IG_CTRL_CLK
17	TP_LVDS_IG_CTRL_DATA	==	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
17	TP_PCH_LVDS_VBG	==	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	==	TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	==	MAKE_BASE=TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	==	MAKE_BASE=TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	==	TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	==	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3

16	TP_CLINK_CLK	==	TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	==	MAKE_BASE=TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	==	MAKE_BASE=TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	==	TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP
38	TP_FW643_SDA	==	TRUE	NC_FW643_SDA
38	TP_FW643_SM	==	MAKE_BASE=TRUE	NC_FW643_SM
38	TP_FW643_TCK	==	TRUE	NC_FW643_TCK
38	TP_FW643_TMS	==	MAKE_BASE=TRUE	NC_FW643_TMS
38	TP_FW643_FW620_L	==	TRUE	NC_FW643_FW620_L
38	TP_FW643_VBUE	==	MAKE_BASE=TRUE	NC_FW643_VBUE
38	TP_FW643_OCR10_CTL	==	TRUE	NC_FW643_OCR10_CTL
38	TP_FW643_AVREG	==	TRUE	NC_FW643_AVREG
38	TP_FW643_TDI	==	MAKE_BASE=TRUE	NC_FW643_TDI

23	TP_XDP_PCH_OBSFN_A<0..1>	==	TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	==	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDP_PCH_HOOK2	==	TRUE	NC_TP_XDP_PCH_HOOK2
23	TP_XDP_PCH_HOOK3	==	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	==	TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	==	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	==	TRUE	NC_TP_XDP_PCH_HOOK5

16	TP_PCH_GPIO64_CLKOUTFLEX0	==	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	==	MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	==	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	==	MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC_NO_TESTS

660	TRUE	NC_FW2_TBPB	40
660	TRUE	NC_FW2_TPNB	40
660	TRUE	NC_FW2_TPBIA	40
660	TRUE	NC_FW2_TTPA	40
660	TRUE	NC_FW2_TPAN	40
660	TRUE	NC_FW0_TBPB	40
660	TRUE	NC_FW0_TPNB	40
660	TRUE	NC_FW0_TTPA	40

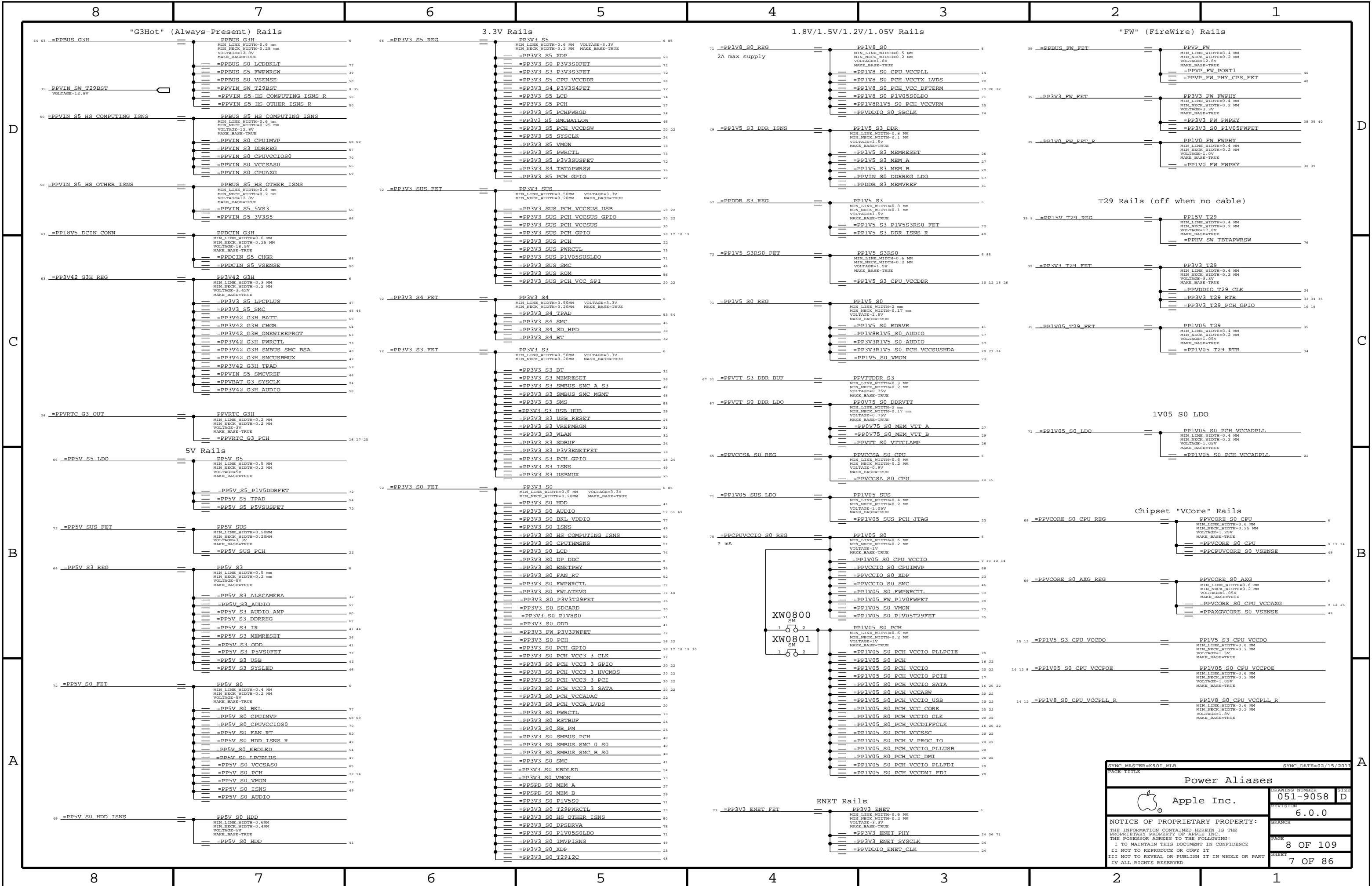
660	TRUE	XDP_PCH_AP_PWR_EN	
660	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	
660	TRUE	XDP_PCH_SDCONN_STATE_RST_L	
660	TRUE	XDP_PCH_ENET_PWR_EN	
660	TRUE	XDP_PCH_SDCONN_DET_L	
660	TRUE	XDP_PCH_S5_PWRGD	23
660	TRUE	XDP_PCH_PWRBTN_L	23
660	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	
660	TRUE	XDP_FW_CLKREQ_L	
660	TRUE	XDP_AP_CLKREQ_L	
660	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	

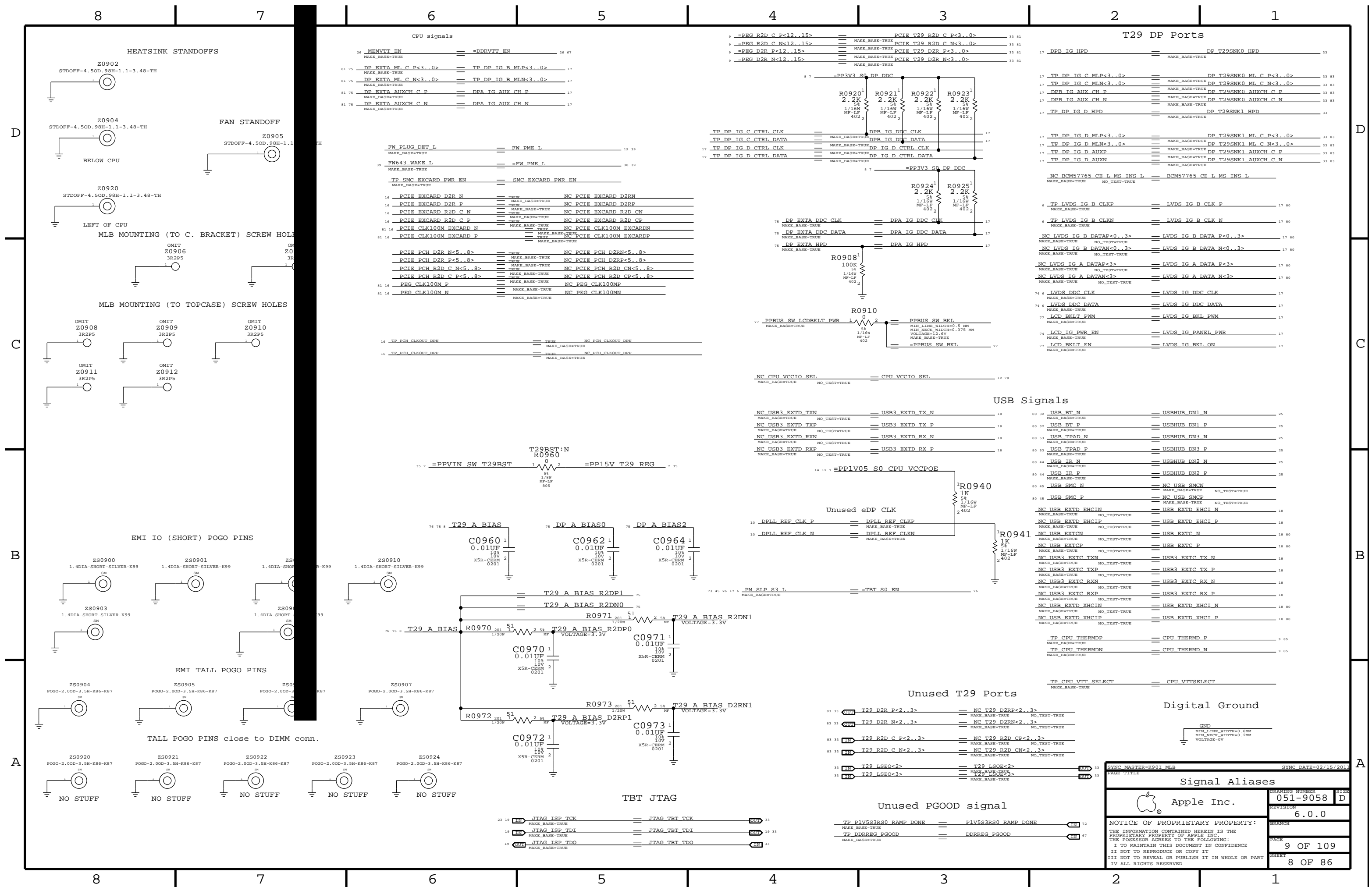
17	TP_SDVO_TVCLKINN	==	TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	==	MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	==	TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	==	MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	==	TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	==	MAKE_BASE=TRUE	NC_SDVO_INTP

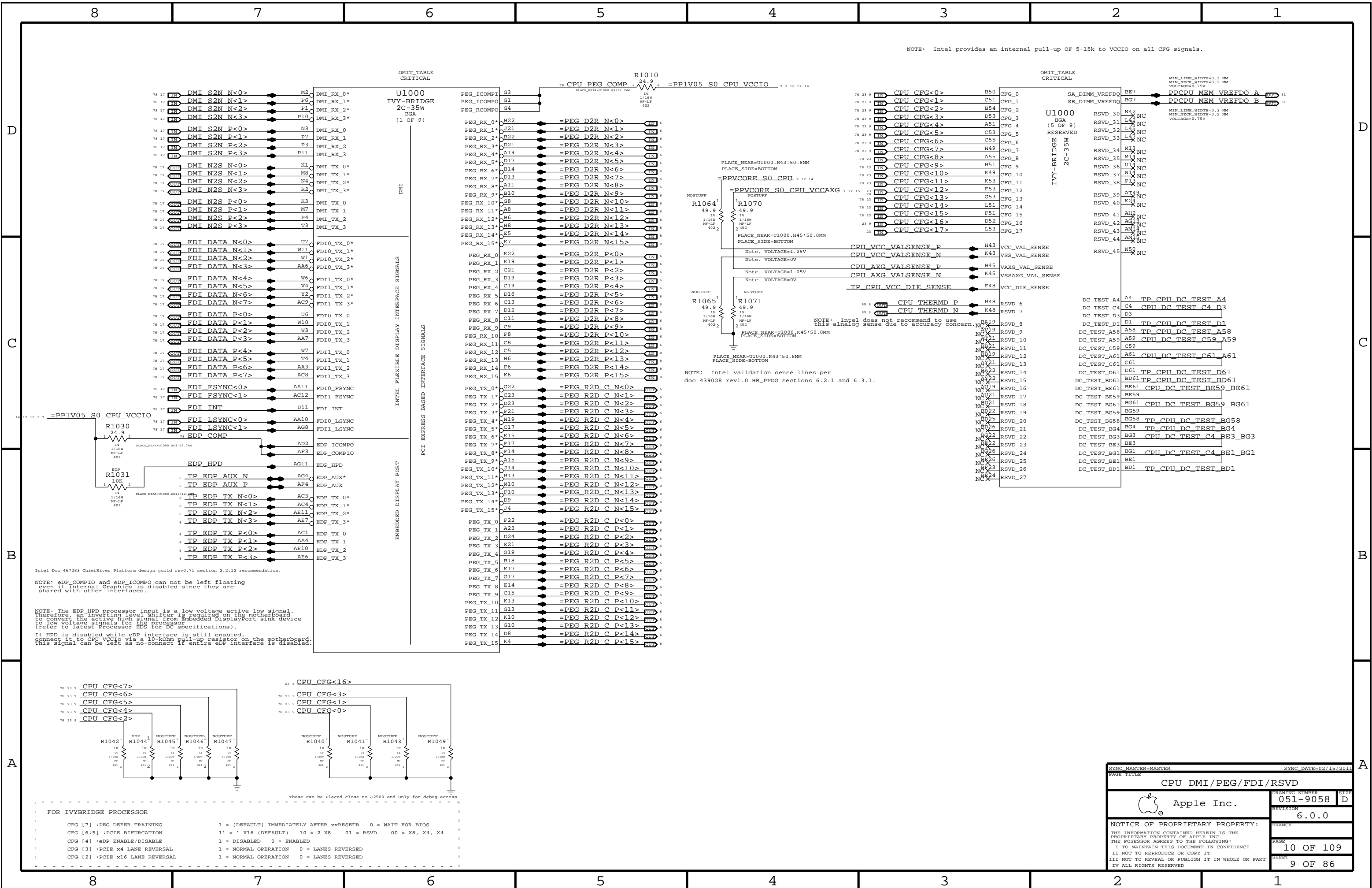
NC_EDP_TXP<0..3>	==	TRUE	TP_EDP_TX_P<0..3>
NC_EDP_TXN<0..3>	==	TRUE	TP_EDP_TX_N<0..3>
NC_EDP_AUXP	==	TRUE	TP_EDP_AUX_P
NC_EDP_AUXN	==	TRUE	TP_EDP_AUX_N
NC_CPU_THERMDA	==	TRUE	TP_CPU_THERMDA
NC_CPU_THERMDC	==	TRUE	TP_CPU_THERMDC
NC_CPU_RSVD<30..45>	==	TRUE	TP_CPU_RSVD<30..45>
NC_CPU_RSVD<8..27>	==	TRUE	TP_CPU_RSVD<8..27>

NC_PEG_R2D_CP<0..7>	==	TRUE	=PEG_R2D_C_P<0..7>
NC_PEG_R2D_CN<0..7>	==	TRUE	=PEG_R2D_C_N<0..7>
NC_PEG_D2RP<0..7>	==	TRUE	=PEG_D2R_P<0..7>
NC_PEG_D2RN<0..7>	==	TRUE	=PEG_D2R_N<0..7>
NC_PEG_R2D_CP<8..11>	==	TRUE	=PEG_R2D_C_P<8..11>
NC_PEG_R2D_CN<8..11>	==	TRUE	=PEG_R2D_C_N<8..11>
NC_PEG_D2RP<8..11>	==	TRUE	=PEG_D2R_P<8..11>
NC_PEG_D2RN<8..11>	==	TRUE	=PEG_D2R_N<8..11>

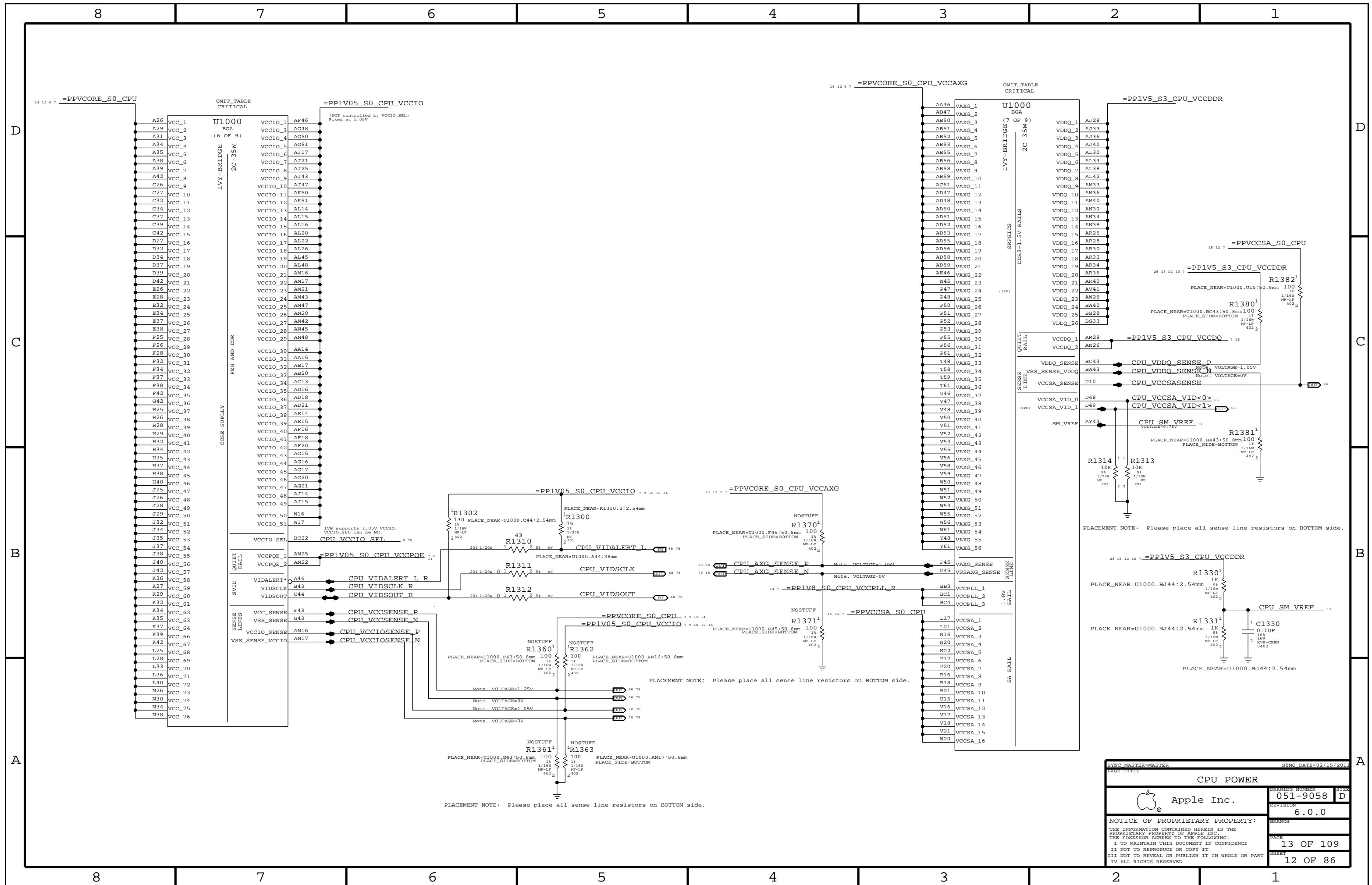
16	TP_PCIE_CLK100M_PEA4N	==	TRUE	NC_PCIE_CLK100M_PEA4N
16	TP_PCIE_CLK100M_PEA4P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEA4P
16	TP_PCIE_CLK100M_PEA5N	==	TRUE	NC_PCIE_CLK100M_PEA5N
16	TP_PCIE_CLK100M_PEA5P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEA5P
16	TP_PCIE_CLK100M_PEA6N	==	TRUE	NC_PCIE_CLK100M_PEA6N
16	TP_PCIE_CLK100M_PEA6P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEA6P
16	TP_PCIE_CLK100M_PEA7N	==	TRUE	NC_PCIE_CLK100M_PEA7N
16	TP_PCIE_CLK100M_PEA7P	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEA7P
63	TP_PSOC_P1_3	==	MAKE_BASE=TRUE	NC_PSOC_P1_3
16	TP_SATA_C_D2RN	==	MAKE_BASE=TRUE	NC_SATA_C_D2RN
16	TP_SATA_C_D2RP	==	MAKE_BASE=TRUE	NC_SATA_C_D2RP
16	TP_SATA_C_R2D_CN	==	MAKE_BASE=TRUE	NC_SATA_C_R2D_CN
16	TP_SATA_C_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_C_R2D_CP
16	TP_SATA_D_D2RN	==	MAKE_BASE=TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	==	MAKE_BASE=TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	==	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	==	MAKE_BASE=TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	==	MAKE_BASE=TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	==	MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	==	MAKE_BASE=TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	==	MAKE_BASE=TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	==	MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	==	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP

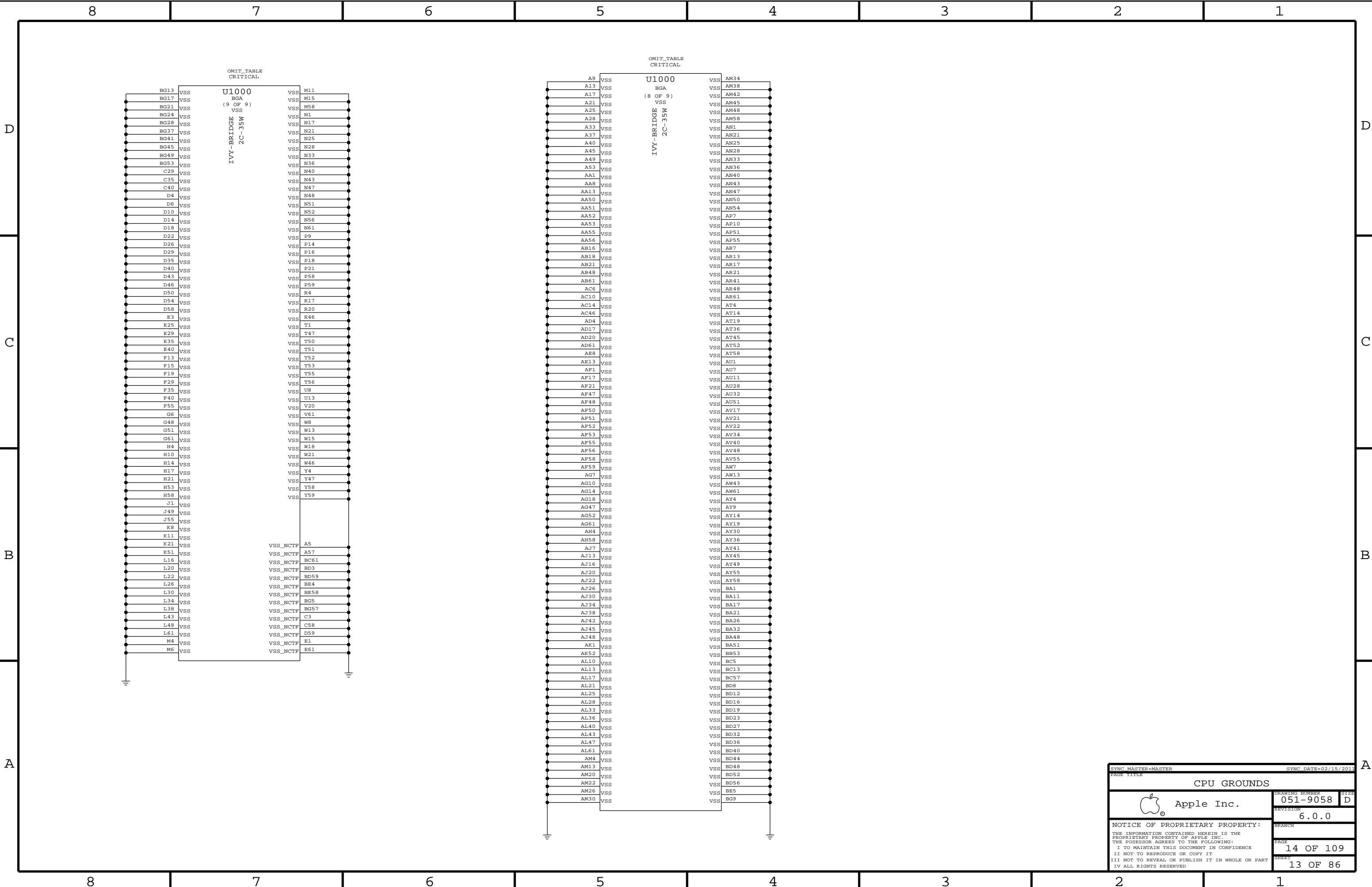






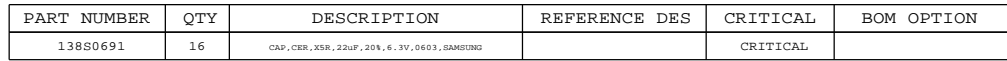
8	7	6	5	4	3	2	1							
D	C	B	A	U1000 BGA (3 OF 9) IVY-BRIDGE 2C-35W MEMORY CHANNEL A				U1000 BGA (4 OF 9) IVY-BRIDGE 2C-35W MEMORY CHANNEL B						
				OMIT_TABLE CRITICAL				OMIT_TABLE CRITICAL						
				79 26 MEM A DO<0> AG6 SA_DQ_0				79 26 MEM B DO<0> AL4 SB_DQ_0						
				79 26 MEM A DO<1> AJ6 SA_DQ_1				79 26 MEM B DO<1> AL1 SB_DQ_1						
				79 26 MEM A DO<2> AP11 SA_DQ_2				79 26 MEM B DO<2> AN3 SB_DQ_2						
				79 26 MEM A DO<3> AL6 SA_DQ_3				79 26 MEM B DO<3> AR4 SB_DQ_3						
				79 26 MEM A DO<4> AJ10 SA_DQ_4				79 26 MEM B DO<4> AK4 SB_DQ_4						
				79 26 MEM A DO<5> AJ8 SA_DQ_5				79 26 MEM B DO<5> AK3 SB_DQ_5						
				79 26 MEM A DO<6> AL8 SA_DQ_6				79 26 MEM B DO<6> AN4 SB_DQ_6						
				79 26 MEM A DO<7> AL7 SA_DQ_7				79 26 MEM B DO<7> AR1 SB_DQ_7						
C	B	A	A	79 26 MEM A DO<8> AR11 SA_DQ_8				79 26 MEM B DO<8> AU4 SB_DQ_8						
				79 26 MEM A DO<9> AP6 SA_DQ_9				79 26 MEM B DO<9> AT2 SB_DQ_9						
				79 26 MEM A DO<10> AU6 SA_DQ_10				79 26 MEM B DO<10> AV4 SB_DQ_10						
				79 26 MEM A DO<11> AV9 SA_DQ_11				79 26 MEM B DO<11> BA4 SB_DQ_11						
				79 26 MEM A DO<12> AR6 SA_DQ_12				79 26 MEM B DO<12> AU3 SB_DQ_12						
				79 26 MEM A DO<13> AP8 SA_DQ_13				79 26 MEM B DO<13> AR3 SB_DQ_13						
				79 26 MEM A DO<14> AT13 SA_DQ_14				79 26 MEM B DO<14> AY2 SB_DQ_14						
				79 26 MEM A DO<15> AU13 SA_DQ_15				79 26 MEM B DO<15> BA3 SB_DQ_15						
				79 26 MEM A DO<16> BC7 SA_DQ_16				79 26 MEM B DO<16> BE9 SB_DQ_16						
				79 26 MEM A DO<17> BB7 SA_DQ_17				79 26 MEM B DO<17> BD9 SB_DQ_17						
B	A	A	A	79 26 MEM A DO<18> BA13 SA_DQ_18				79 26 MEM B DO<18> BD13 SB_DQ_18						
				79 26 MEM A DO<19> BB11 SA_DQ_19				79 26 MEM B DO<19> BF12 SB_DQ_19						
				79 26 MEM A DO<20> BA7 SA_DQ_20				79 26 MEM B DO<20> BF8 SB_DQ_20						
				79 26 MEM A DO<21> BA9 SA_DQ_21				79 26 MEM B DO<21> BD10 SB_DQ_21						
				79 26 MEM A DO<22> BB9 SA_DQ_22				79 26 MEM B DO<22> BD14 SB_DQ_22						
				79 26 MEM A DO<23> AV13 SA_DQ_23				79 26 MEM B DO<23> BE13 SB_DQ_23						
				79 26 MEM A DO<24> AV14 SA_DQ_24				79 26 MEM B DO<24> BF16 SB_DQ_24						
				79 26 MEM A DO<25> AR14 SA_DQ_25				79 26 MEM B DO<25> BE17 SB_DQ_25						
				79 26 MEM A DO<26> AY17 SA_DQ_26				79 26 MEM B DO<26> BE18 SB_DQ_26						
				79 26 MEM A DO<27> AR19 SA_DQ_27				79 26 MEM B DO<27> BE21 SB_DQ_27						
A	A	A	A	79 26 MEM A DO<28> BA14 SA_DQ_28				79 26 MEM B DO<28> BE14 SB_DQ_28						
				79 26 MEM A DO<29> AU14 SA_DQ_29				79 26 MEM B DO<29> BG14 SB_DQ_29						
				79 26 MEM A DO<30> BB14 SA_DQ_30				79 26 MEM B DO<30> BG18 SB_DQ_30						
				79 26 MEM A DO<31> BB17 SA_DQ_31				79 26 MEM B DO<31> BF19 SB_DQ_31						
				79 26 MEM A DO<32> BA45 SA_DQ_32				79 26 MEM B DO<32> BD50 SB_DQ_32						
				79 26 MEM A DO<33> AR43 SA_DQ_33				79 26 MEM B DO<33> BF48 SB_DQ_33						
				79 26 MEM A DO<34> AW48 SA_DQ_34				79 26 MEM B DO<34> BD53 SB_DQ_34						
				79 26 MEM A DO<35> BC48 SA_DQ_35				79 26 MEM B DO<35> BF52 SB_DQ_35						
				79 26 MEM A DO<36> BC45 SA_DQ_36				79 26 MEM B DO<36> BD49 SB_DQ_36						
				79 26 MEM A DO<37> AR45 SA_DQ_37				79 26 MEM B DO<37> BE49 SB_DQ_37						
				79 26 MEM A DO<38> AT48 SA_DQ_38				79 26 MEM B DO<38> BD54 SB_DQ_38						
				79 26 MEM A DO<39> AY48 SA_DQ_39				79 26 MEM B DO<39> BE53 SB_DQ_39						
				79 26 MEM A DO<40> BA49 SA_DQ_40				79 26 MEM B DO<40> BF56 SB_DQ_40						
				79 26 MEM A DO<41> AV49 SA_DQ_41				79 26 MEM B DO<41> BE57 SB_DQ_41						
				79 26 MEM A DO<42> BB51 SA_DQ_42				79 26 MEM B DO<42> BC59 SB_DQ_42						
				79 26 MEM A DO<43> AY53 SA_DQ_43				79 26 MEM B DO<43> AY60 SB_DQ_43						
				79 26 MEM A DO<44> BB49 SA_DQ_44				79 26 MEM B DO<44> BE54 SB_DQ_44						
				79 26 MEM A DO<45> AU49 SA_DQ_45				79 26 MEM B DO<45> BG54 SB_DQ_45						
				79 26 MEM A DO<46> BA53 SA_DQ_46				79 26 MEM B DO<46> BA58 SB_DQ_46						
				79 26 MEM A DO<47> BB55 SA_DQ_47				79 26 MEM B DO<47> AW59 SB_DQ_47						
				79 26 MEM A DO<48> BA55 SA_DQ_48				79 26 MEM B DO<48> AW58 SB_DQ_48						
				79 26 MEM A DO<49> AV56 SA_DQ_49				79 26 MEM B DO<49> AU58 SB_DQ_49						
				79 26 MEM A DO<50> AP50 SA_DQ_50				79 26 MEM B DO<50> AN61 SB_DQ_50						
				79 26 MEM A DO<51> AP53 SA_DQ_51				79 26 MEM B DO<51> AN59 SB_DQ_51						
				79 26 MEM A DO<52> AV54 SA_DQ_52				79 26 MEM B DO<52> AU59 SB_DQ_52						
				79 26 MEM A DO<53> AT54 SA_DQ_53				79 26 MEM B DO<53> AU61 SB_DQ_53						
				79 26 MEM A DO<54> AP56 SA_DQ_54				79 26 MEM B DO<54> AN58 SB_DQ_54						
				79 26 MEM A DO<55> AP52 SA_DQ_55				79 26 MEM B DO<55> AR58 SB_DQ_55						
				79 26 MEM A DO<56> AN57 SA_DQ_56				79 26 MEM B DO<56> AK58 SB_DQ_56						
				79 26 MEM A DO<57> AN53 SA_DQ_57				79 26 MEM B DO<57> AL58 SB_DQ_57						
				79 26 MEM A DO<58> AG56 SA_DQ_58				79 26 MEM B DO<58> AG58 SB_DQ_58						
				79 26 MEM A DO<59> AG53 SA_DQ_59				79 26 MEM B DO<59> AG59 SB_DQ_59						
				79 26 MEM A DO<60> AN55 SA_DQ_60				79 26 MEM B DO<60> AM60 SB_DQ_60						
				79 26 MEM A DO<61> AN52 SA_DQ_61				79 26 MEM B DO<61> AL59 SB_DQ_61						
				79 26 MEM A DO<62> AG55 SA_DQ_62				79 26 MEM B DO<62> AF61 SB_DQ_62						
				79 26 MEM A DO<63> AK56 SA_DQ_63				79 26 MEM B DO<63> AH60 SB_DQ_63						
				79 27 MEM A BA<0> BD37 SA_BS_0				79 27 MEM B BA<0> BG39 SB_BS_0						
				79 27 MEM A BA<1> BF36 SA_BS_1				79 27 MEM B BA<1> BD42 SB_BS_1						
				79 27 MEM A BA<2> BA28 SA_BS_2				79 27 MEM B BA<2> AT22 SB_BS_2						
				79 27 MEM A CAS L BE39 SA_CAS*				79 27 MEM B CAS L AV43 SB_CAS*						
				79 27 MEM A RAS L BD39 SA_RAS*				79 27 MEM B RAS L BF40 SB_RAS*						
				79 27 MEM A WE L AT40 SA_WE*				79 27 MEM B WE L BD40 SB_WE*						





Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

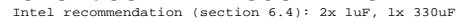


Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

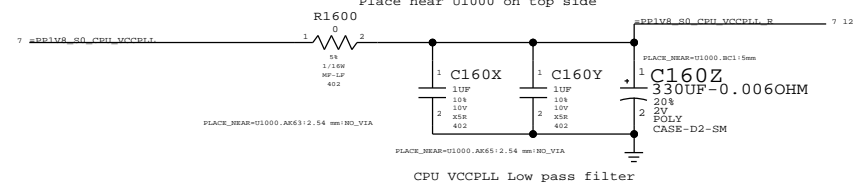
PLACEMENT_NOTE (C1684-C167F):

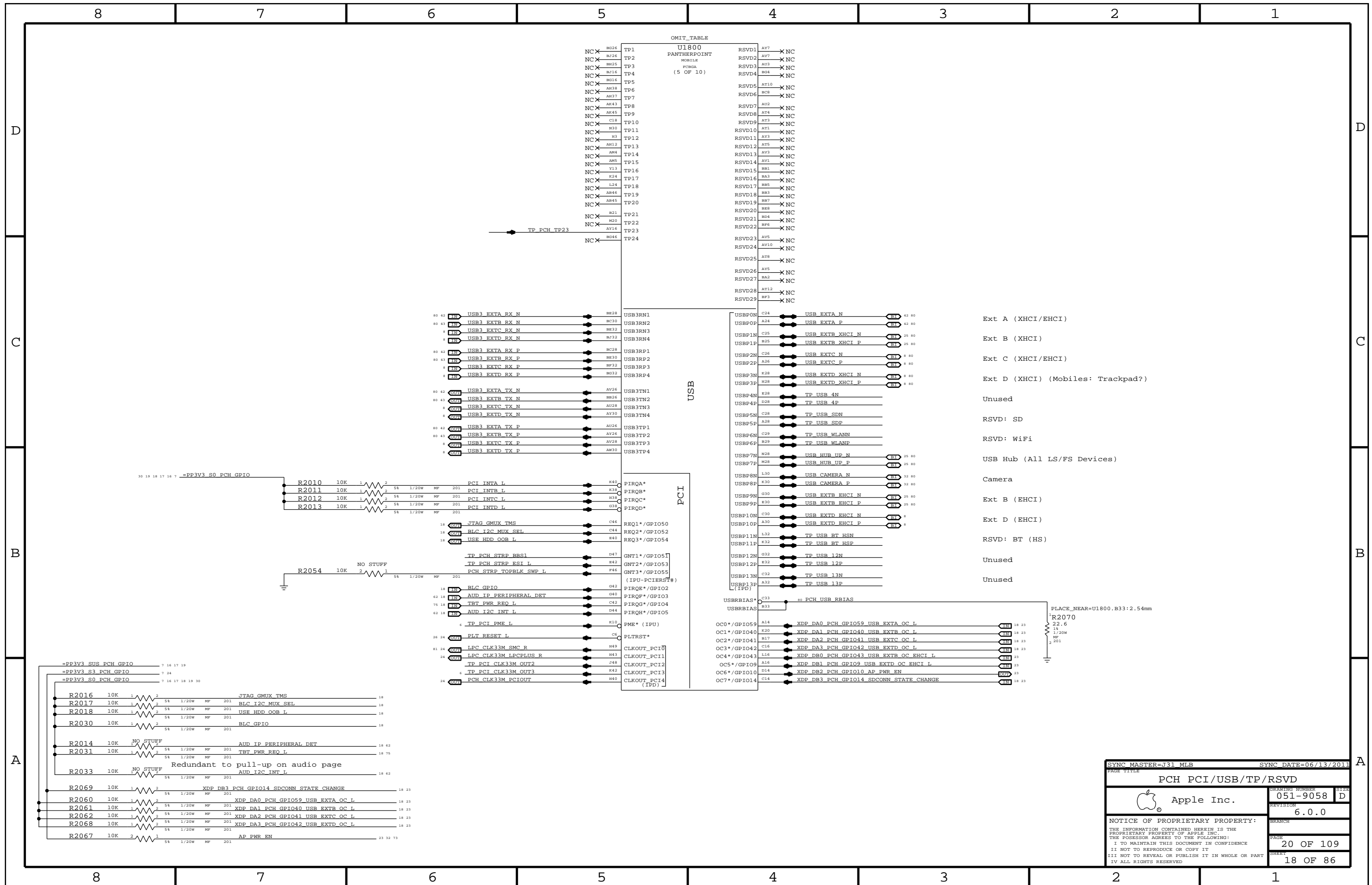
Place on bottom side of U1000

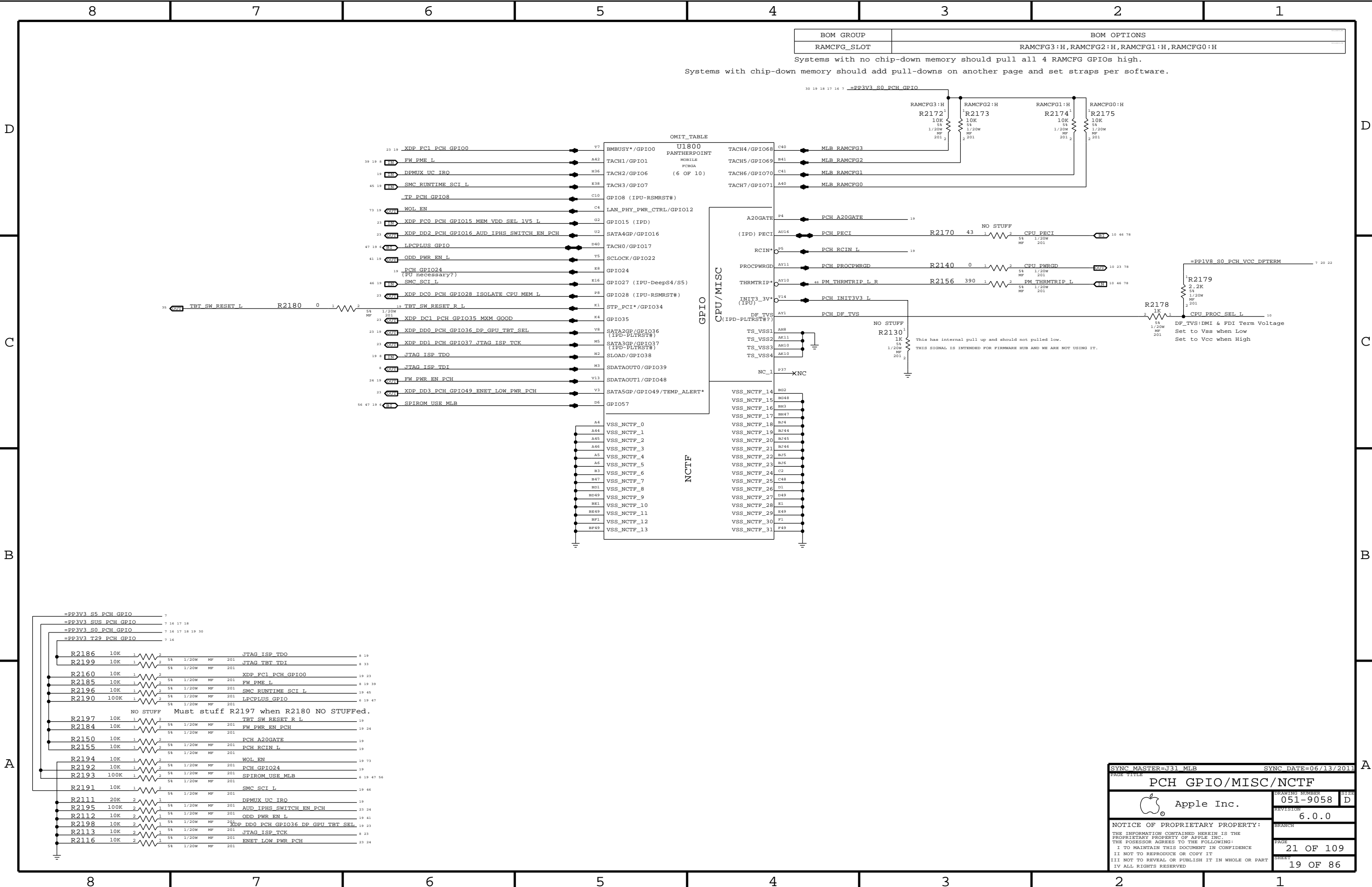


PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side







BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

SYNC MASTER=J31_MLB

SYNC DATE=06/13/2011

PCH GPIO/MISC/NCTF

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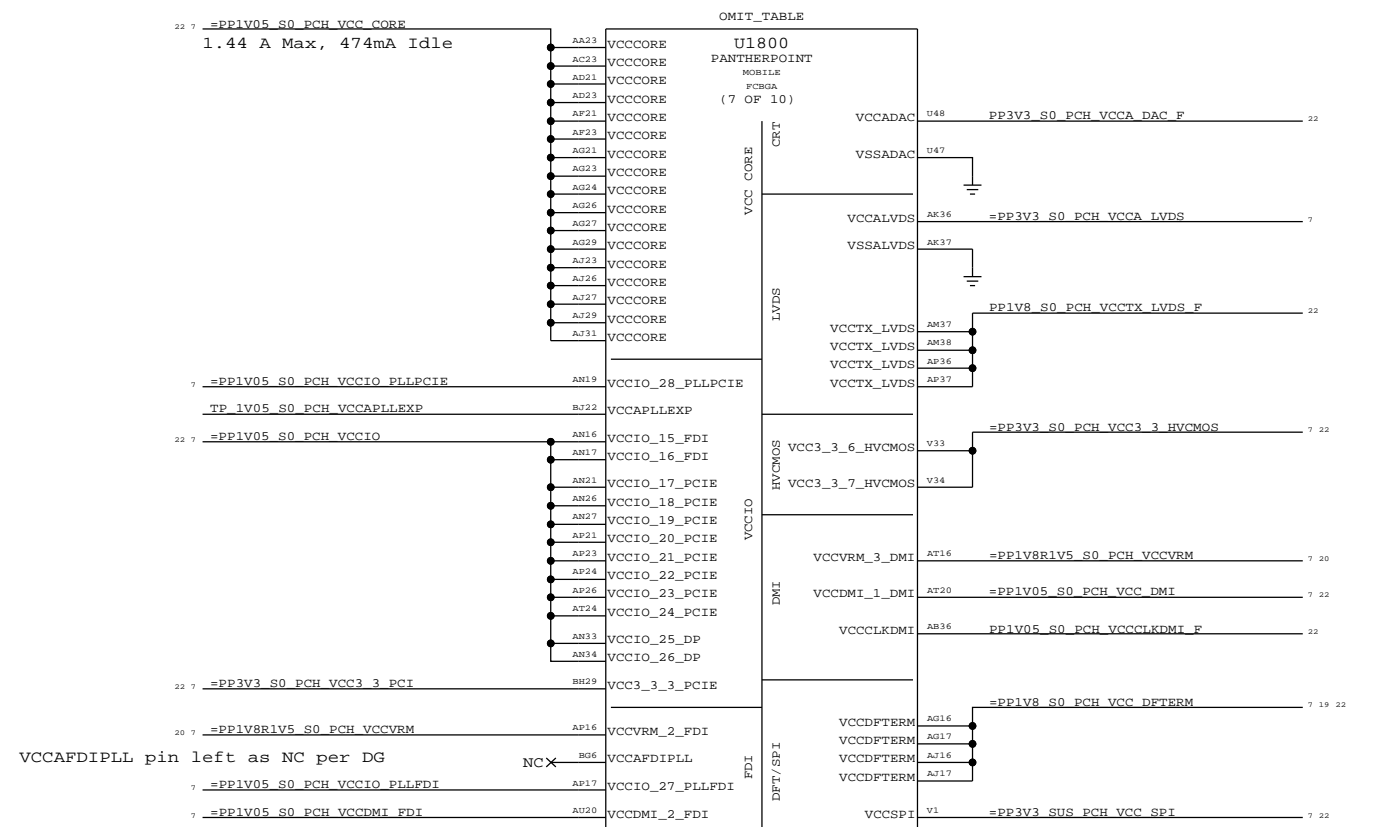
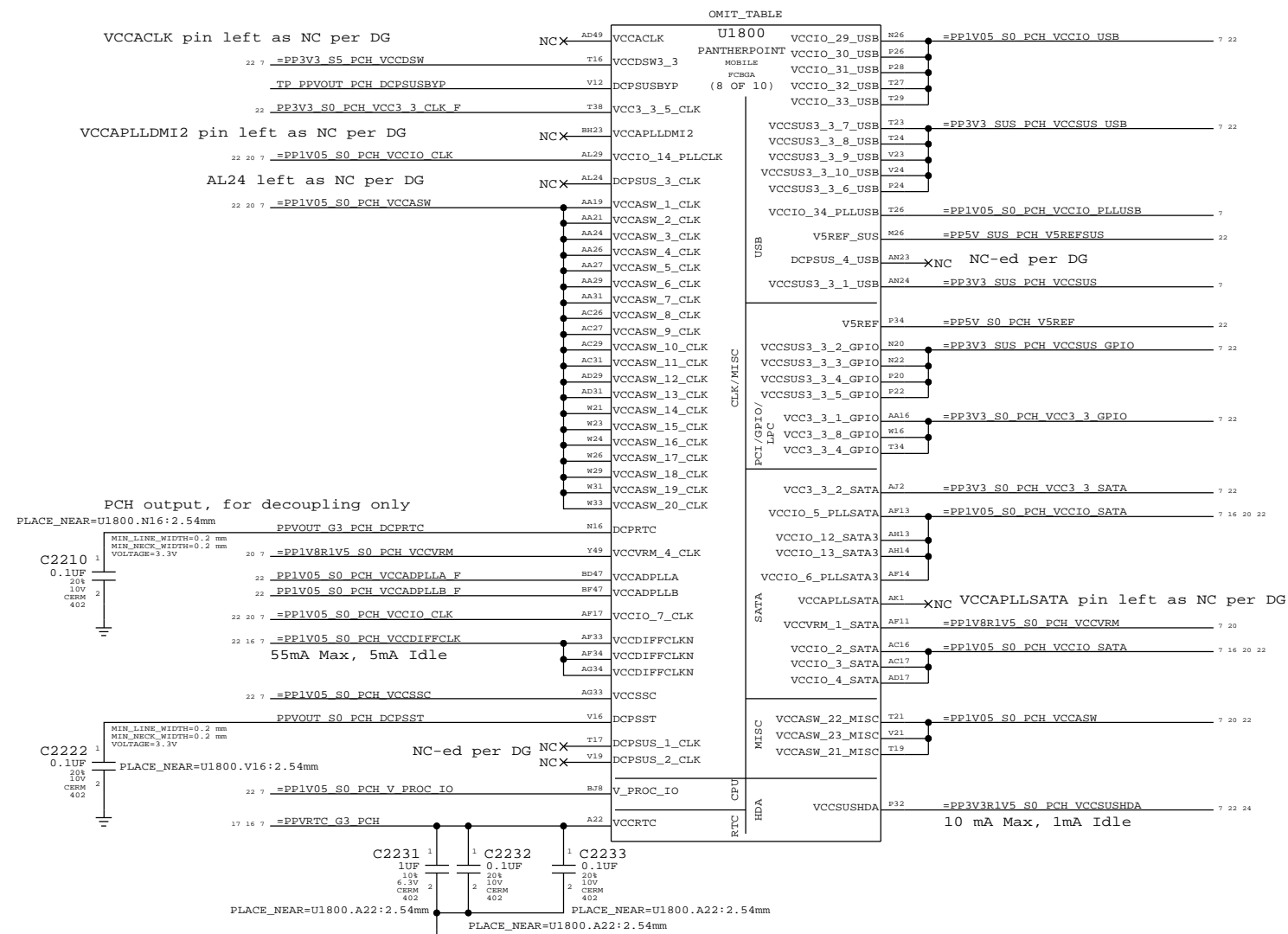
6.0.0

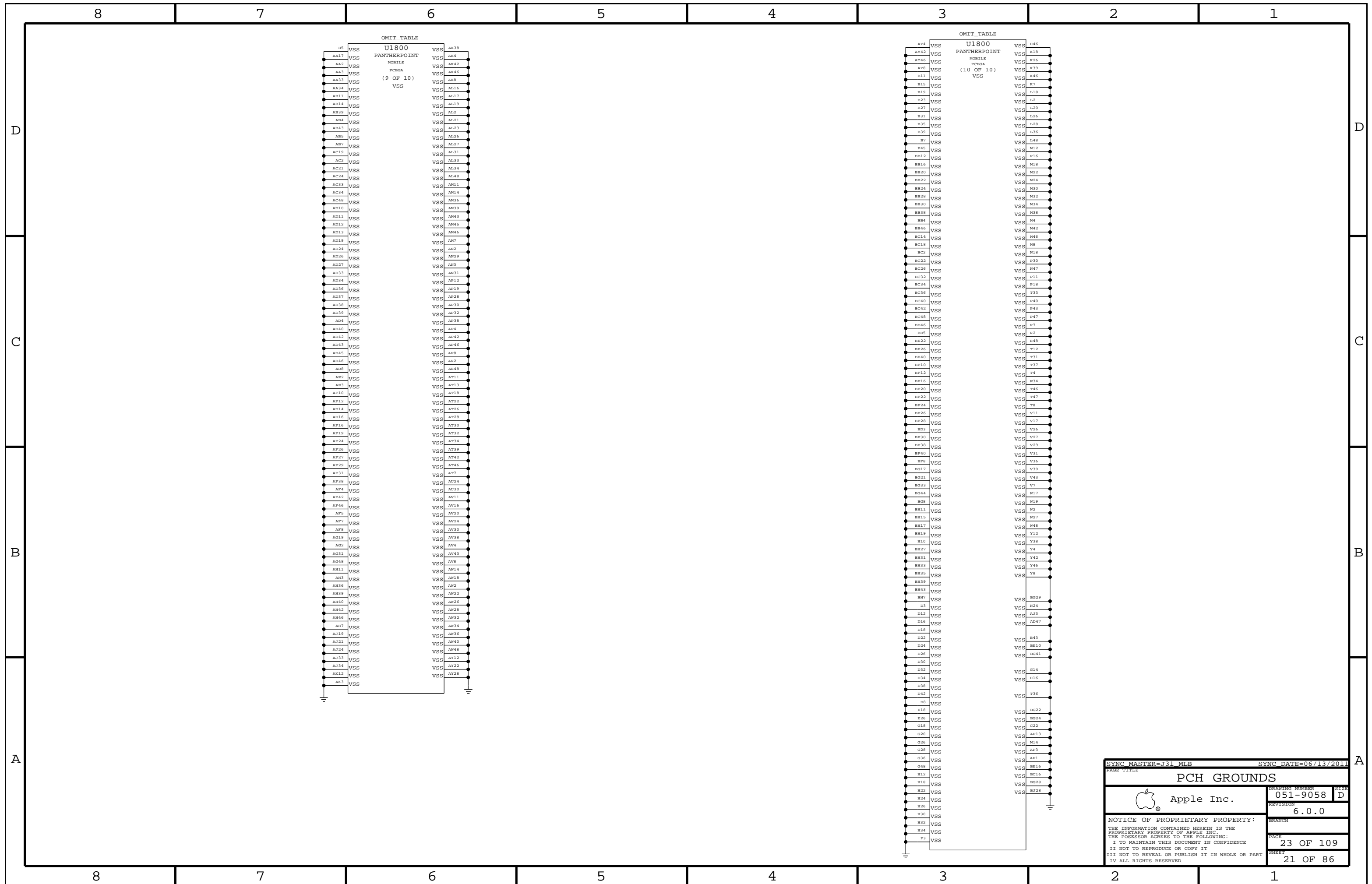
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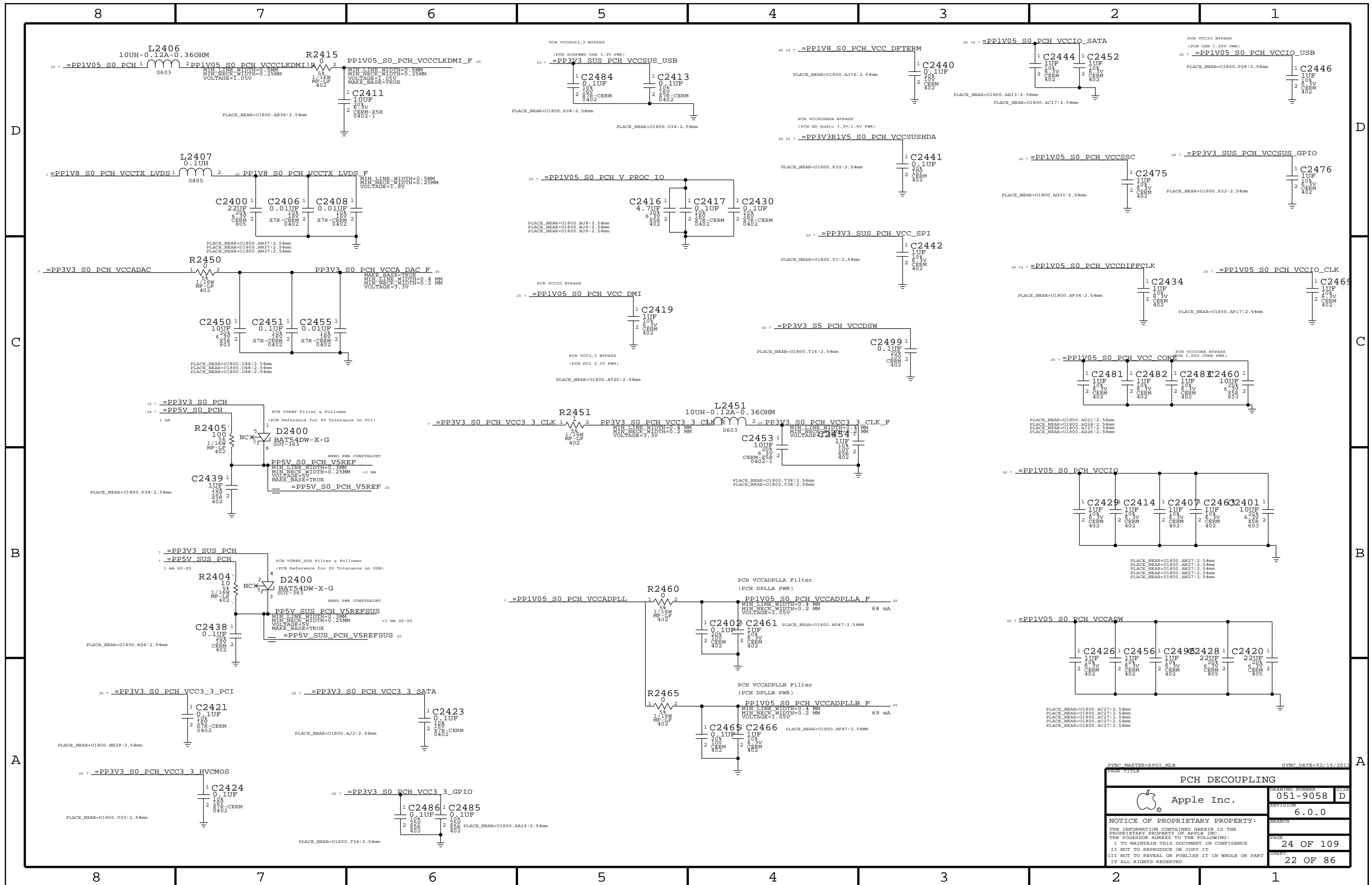
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SHEET

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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

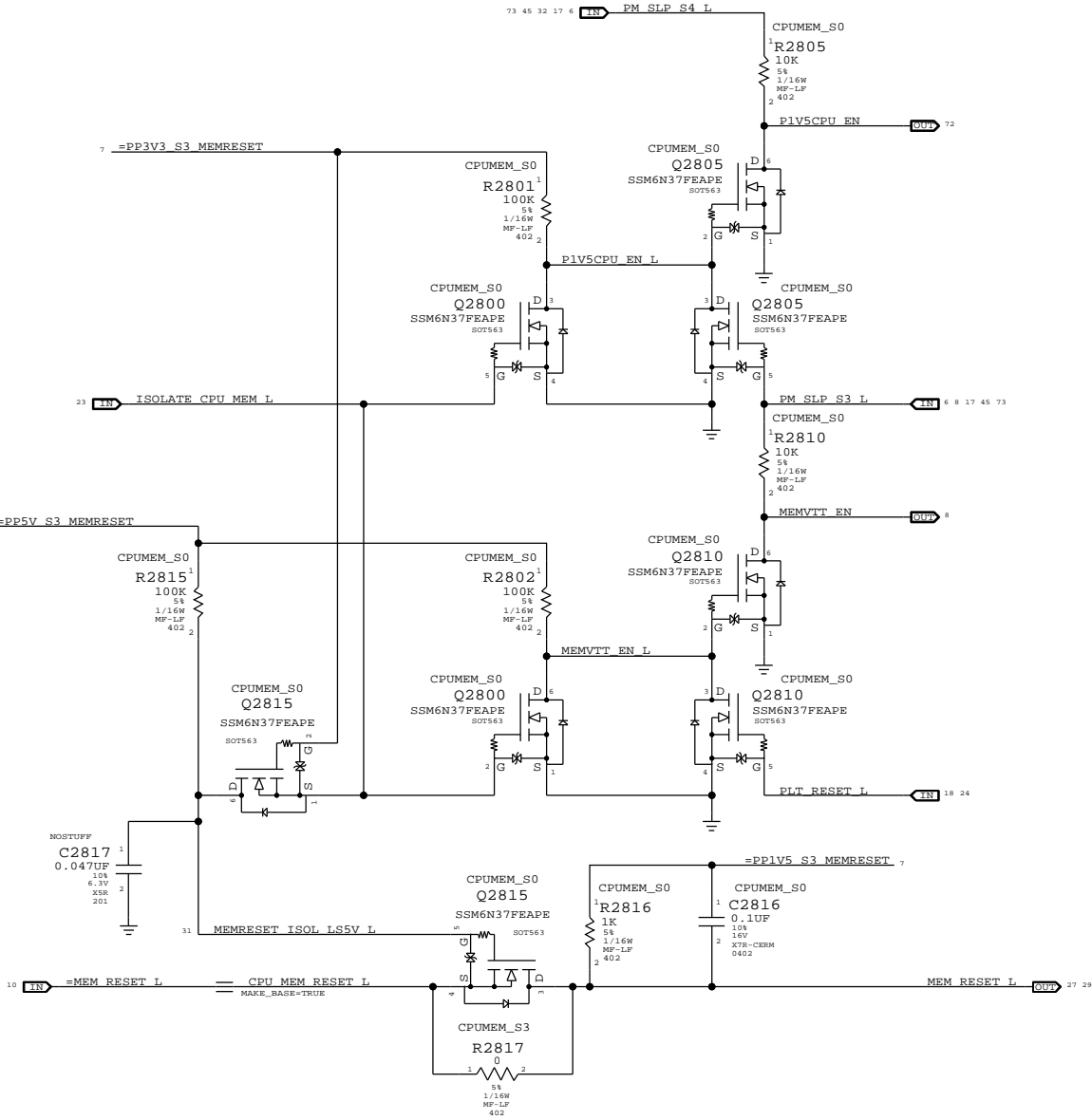
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

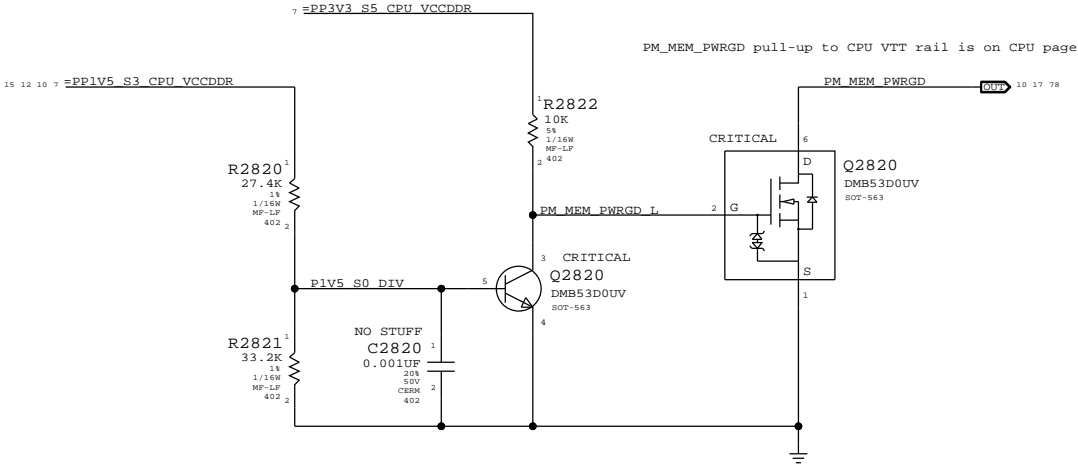
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

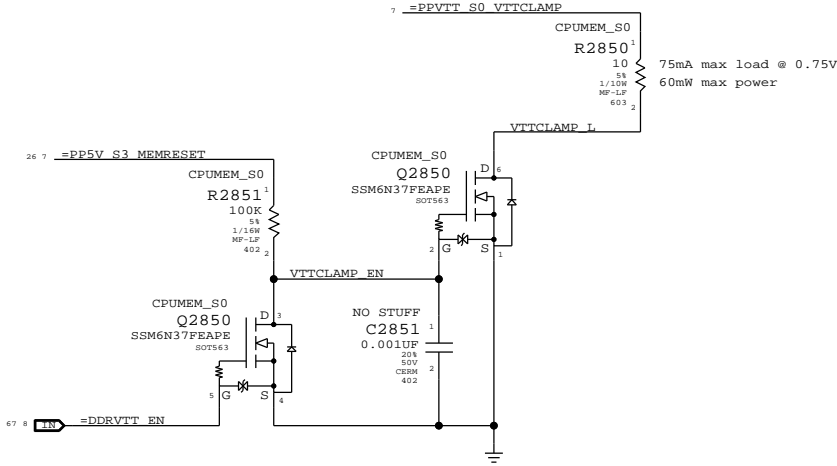


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

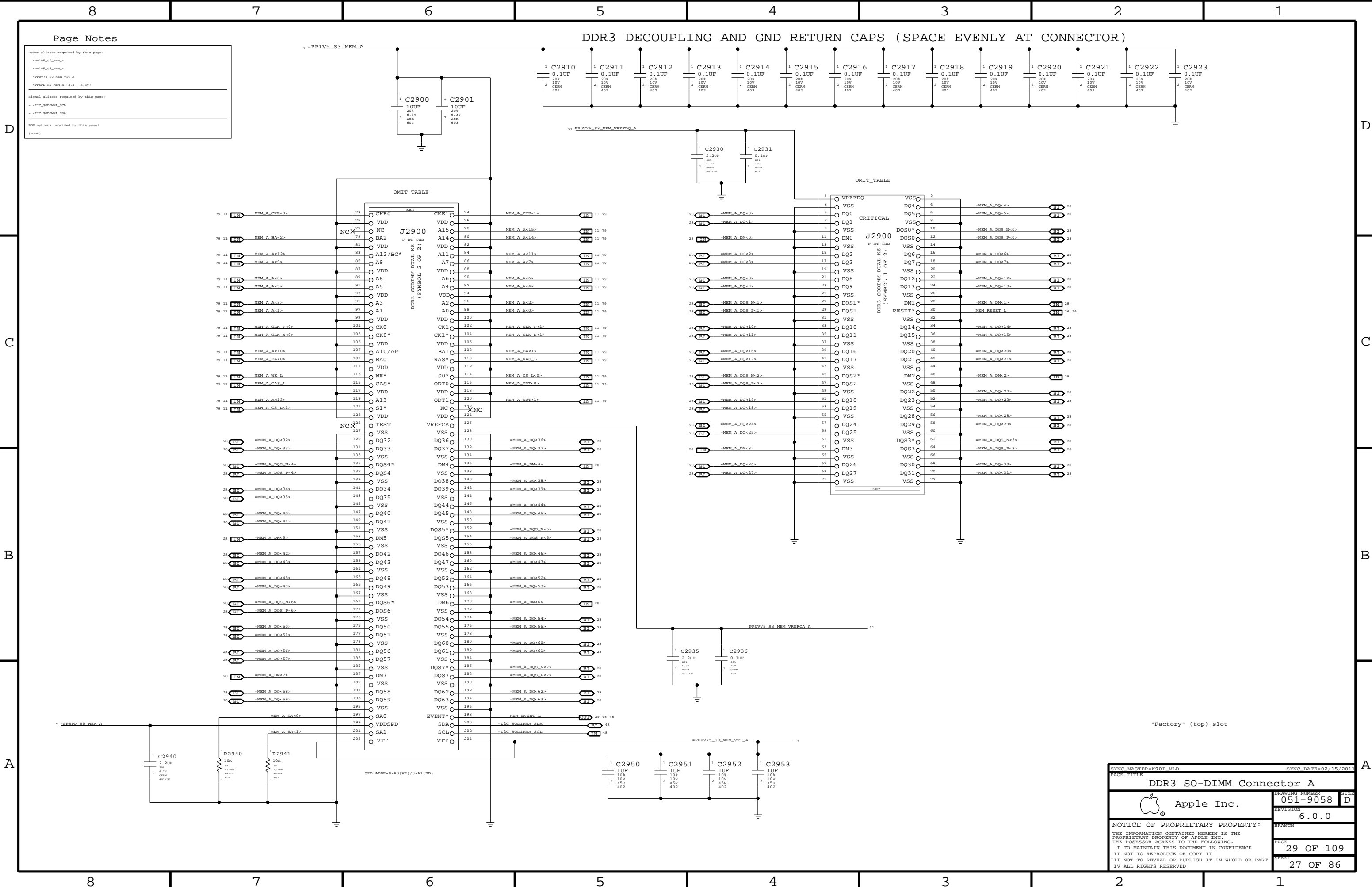


Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
CPU Memory S3 Support			
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		SIZE	D
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		BRANCH	
		PAGE	28 OF 109
		SHEET	26 OF 86



Page Notes

Power aliases required by this page:

- PP1V5_S3_MEM_A
- PP1V5_S3_MEM_A
- PP0V75_S3_MEM_VTT_A
- PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_S0D1MMA_SCL
- I2C_S0D1MMA_SDA

DOM options provided by this page:

(None)

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2011

DDR3 SO-DIMM Connector A

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051-9058

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[illegible]

Page Notes

Power aliases required by this page:
 ~PP1V5_S3_MEM_B
 ~PP1V5_S3_MEM_B
 ~PP0V75_S3_MEM_VTT_B
 ~PPSPD_S0_MEM_B (2.5 - 3.3V)
 Signal aliases required by this page:
 ~I2C_S0D1MMB_SCL
 ~I2C_S0D1MMB_SDA
 ROM options provided by this page:
 (None)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

D

D

C

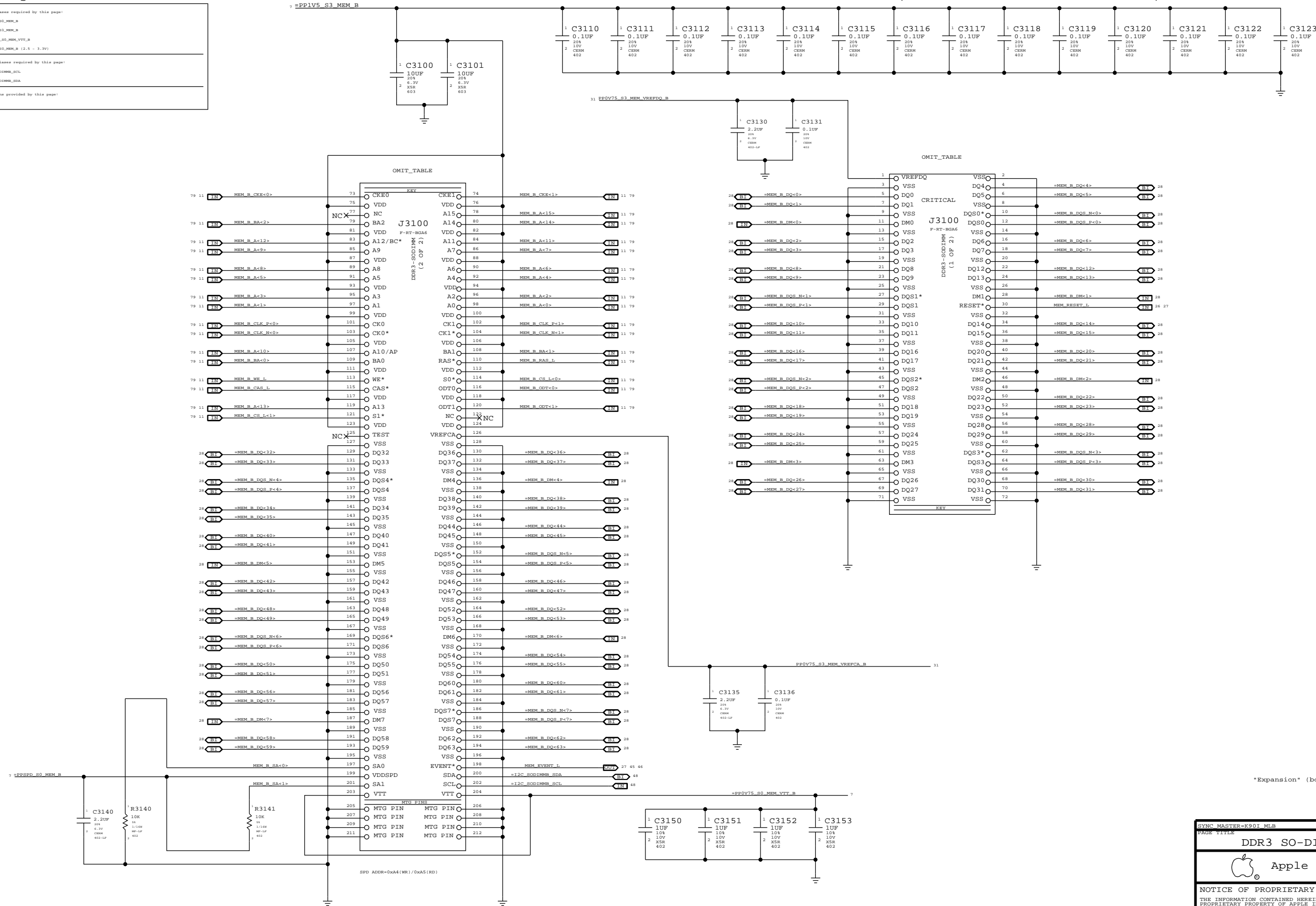
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B

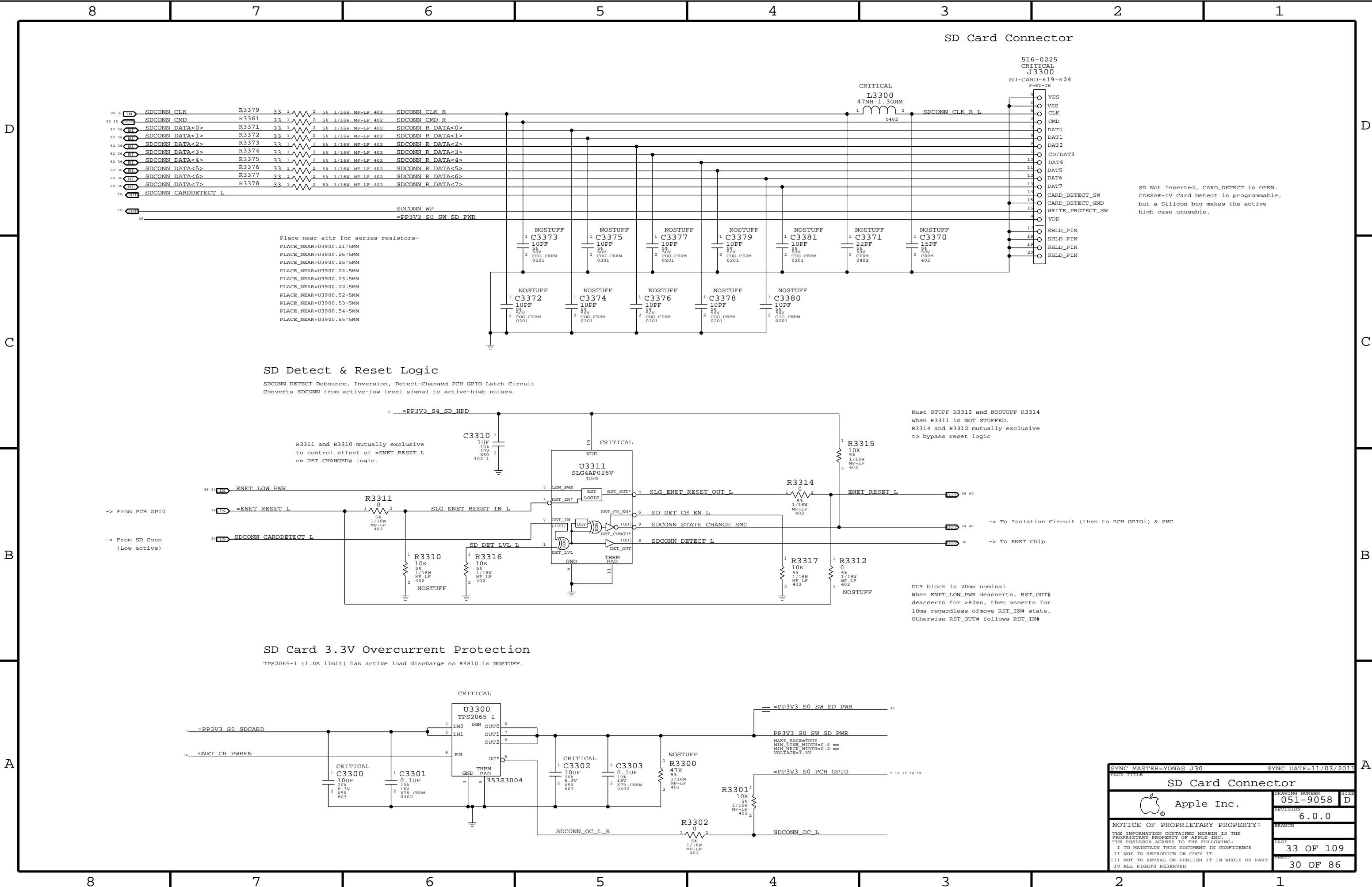
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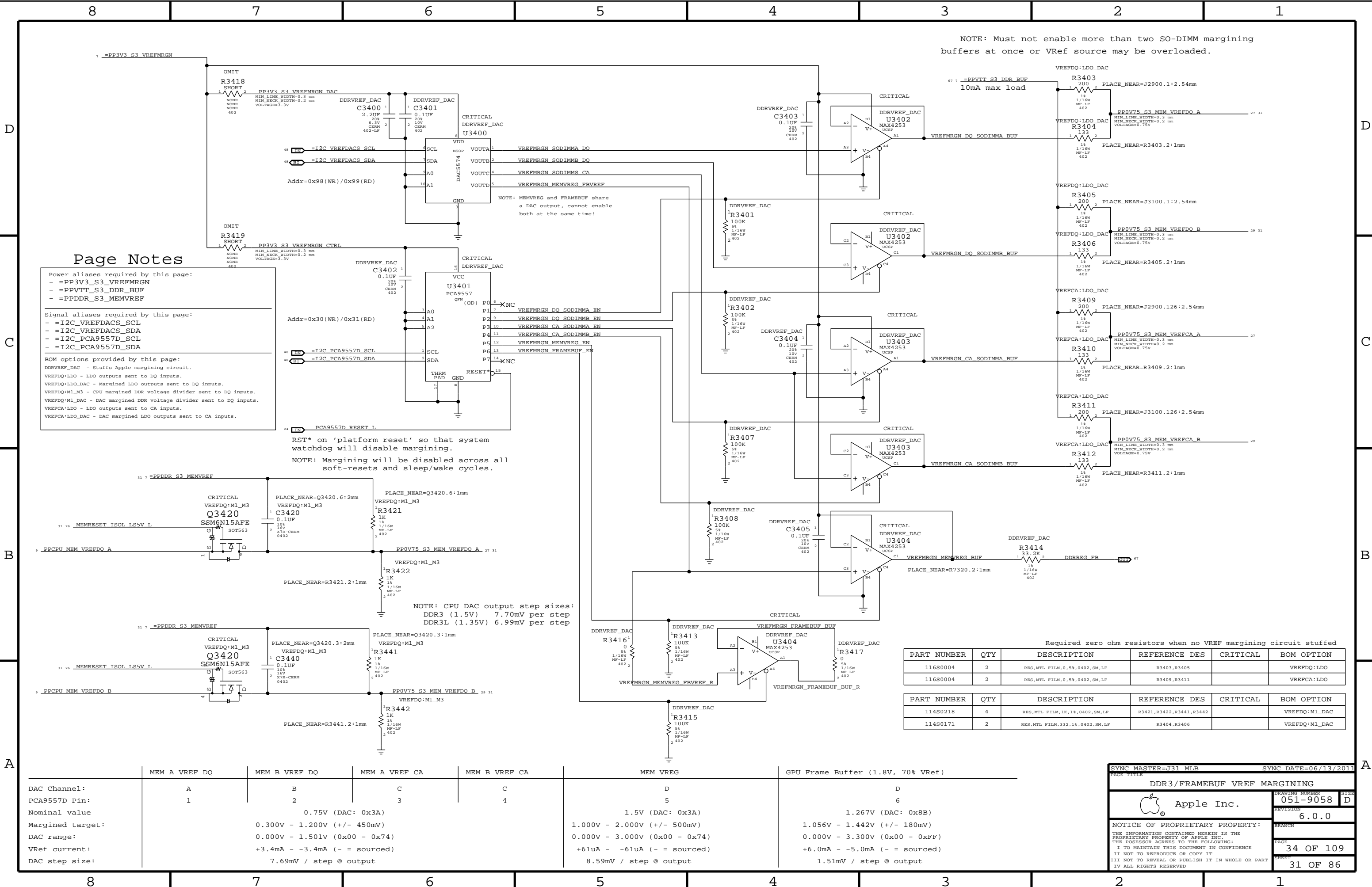
A



"Expansion" (bottom) slot

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DDR3 SO-DIMM Connector B			
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1%,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.000V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J31 MLB

SYNC DATE=06/13/2011

DDR3/FRAMEBUF VREF MARGINING

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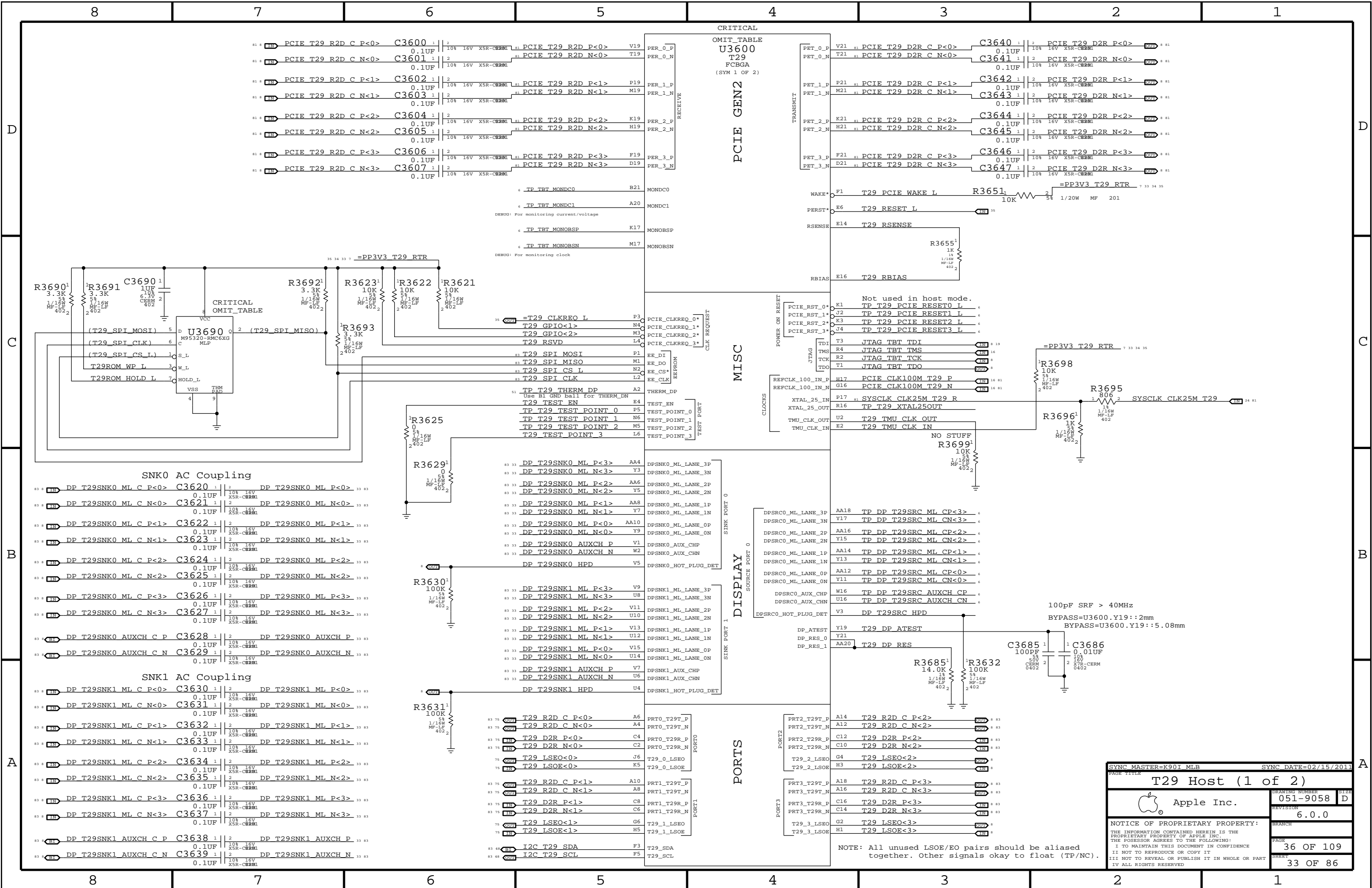
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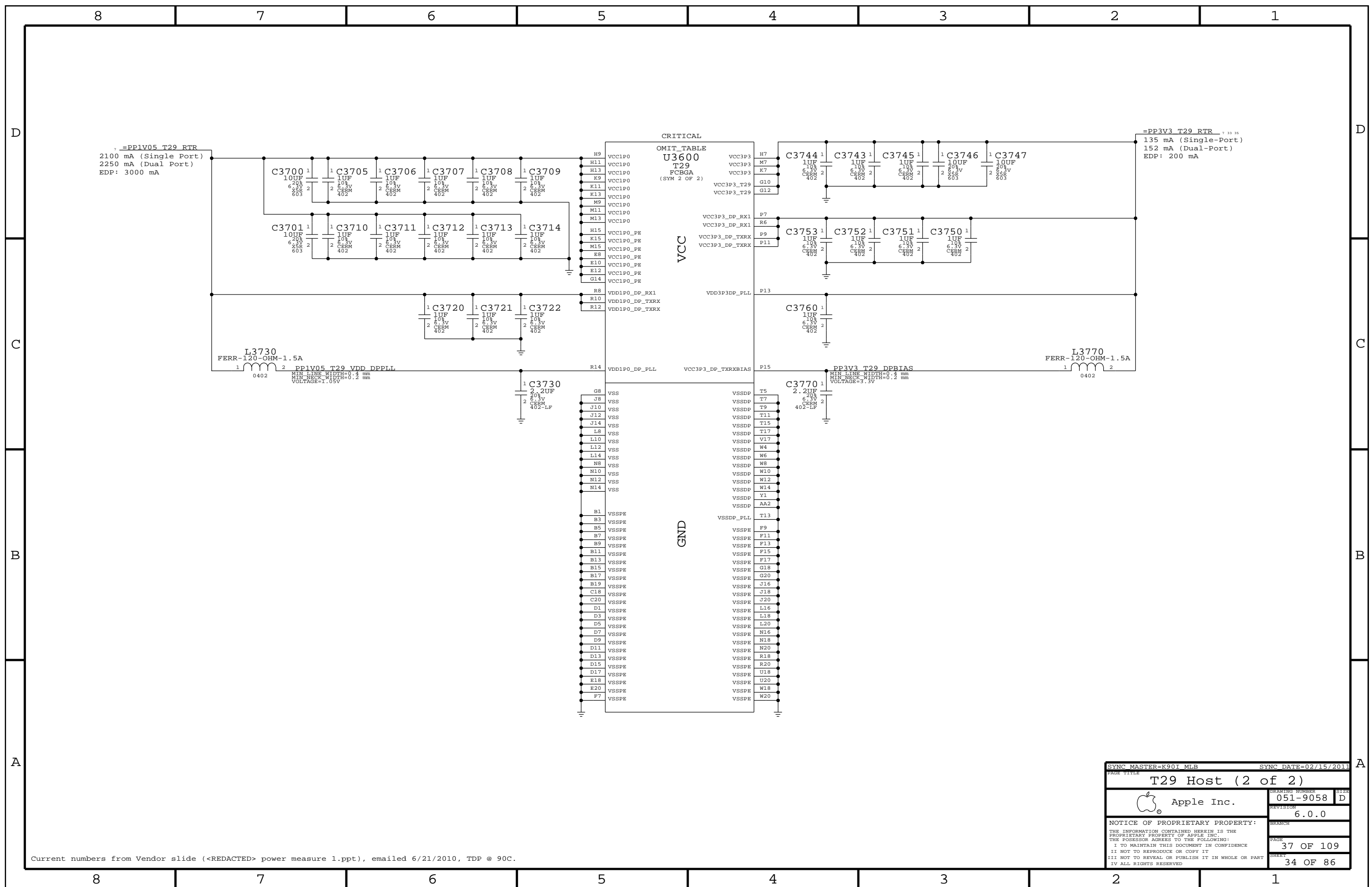
B

B

A

A





8	7	6	5	4	3	2	1
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D


C

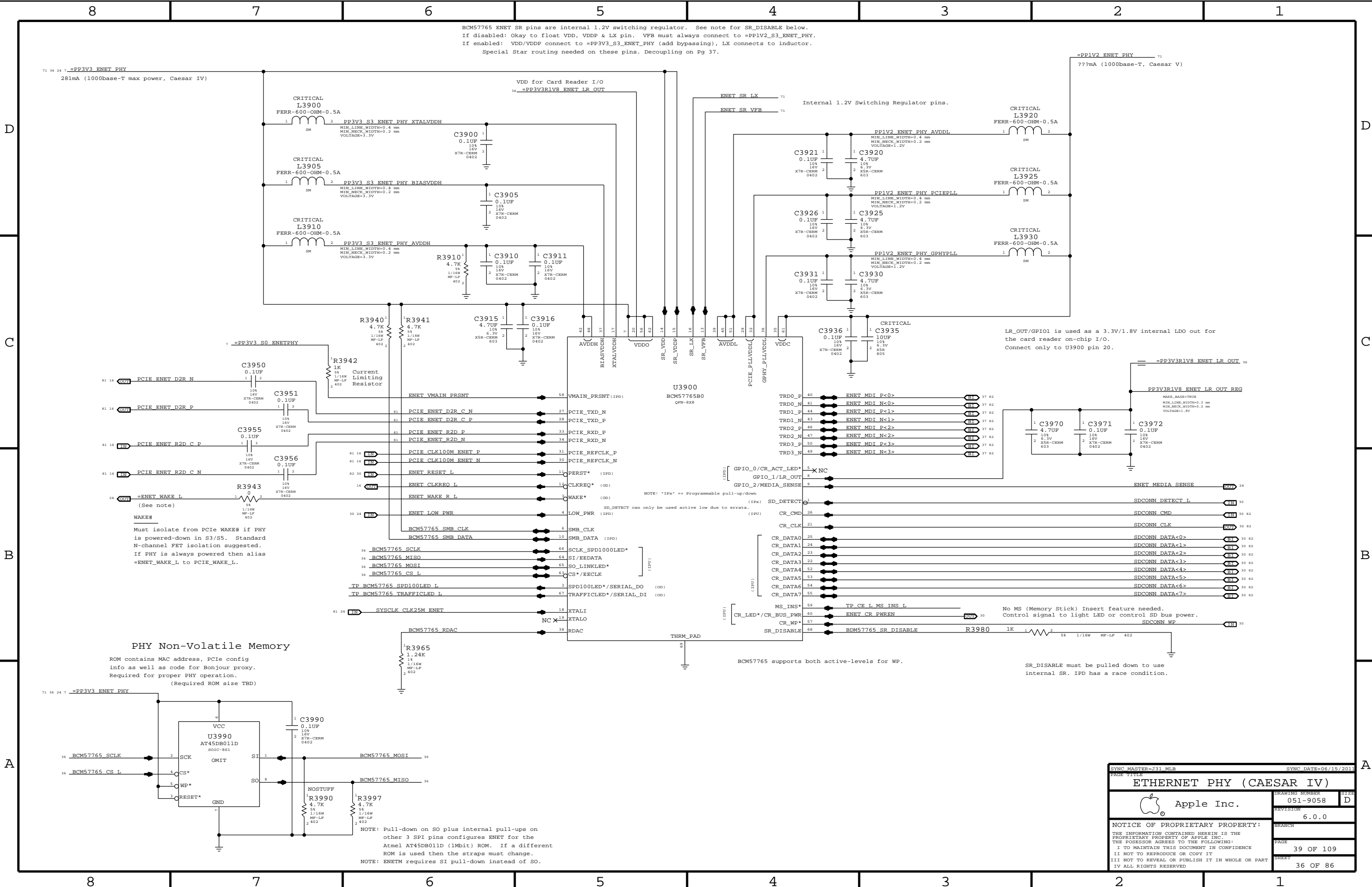
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A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

A

SYNC MASTER-K901 MLB		SYNC DATE=02/15/201	
PAGE TITLE			
T29 Power Support			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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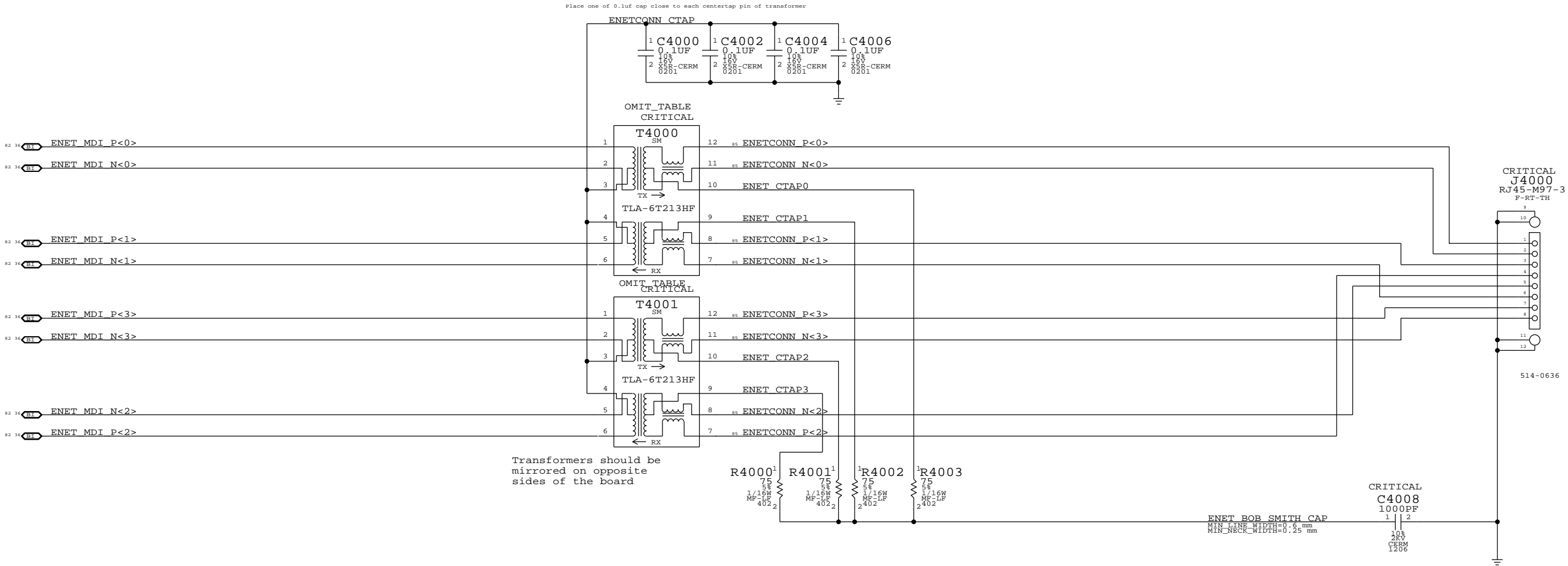


Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
157S0084	2	XFMR, ISO, HALF-PORT, 1000T, 12P, SMD, HF	T4000, T4001	CRITICAL	

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2013

Ethernet Connector

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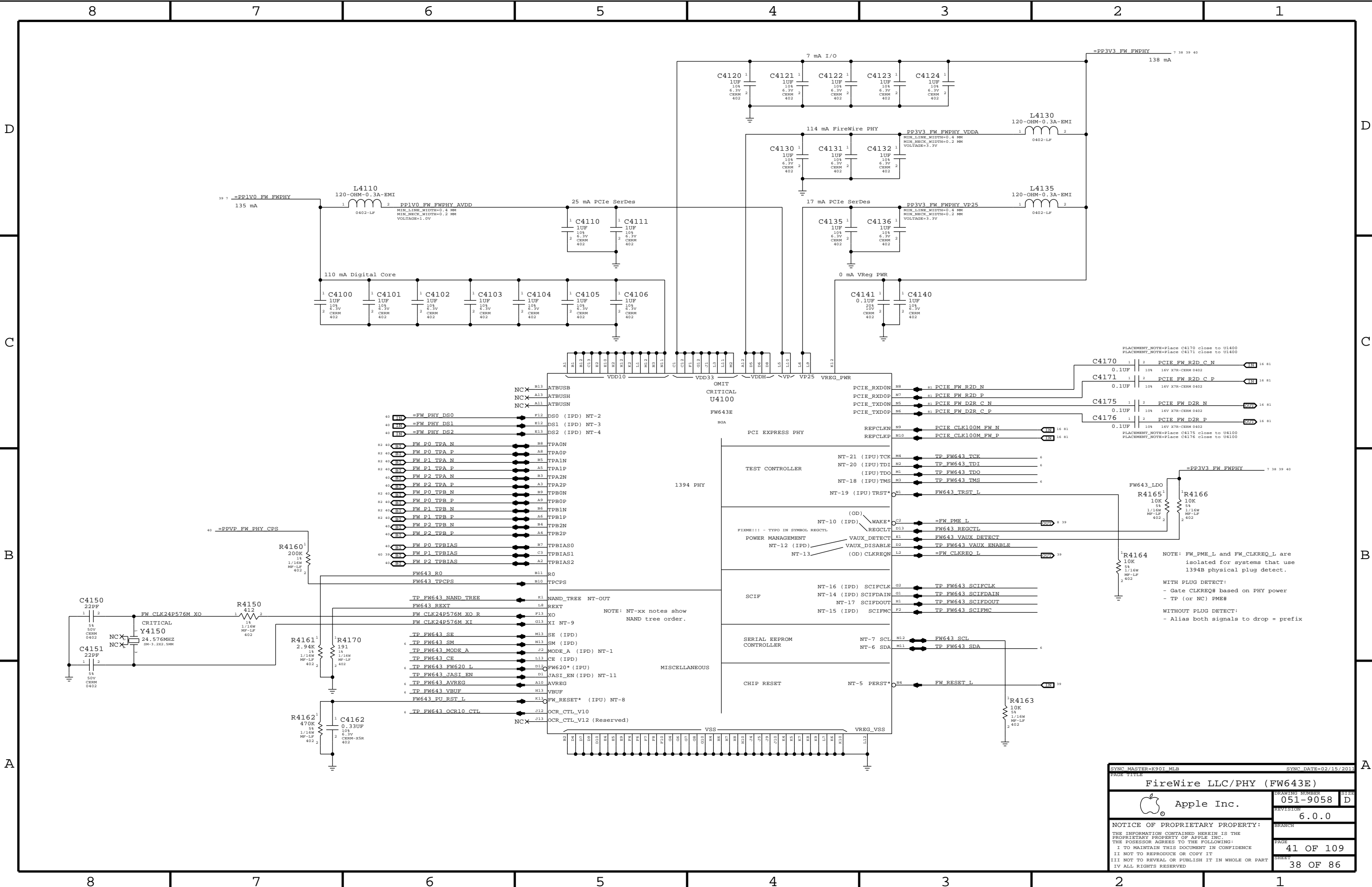
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6.0.0

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Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

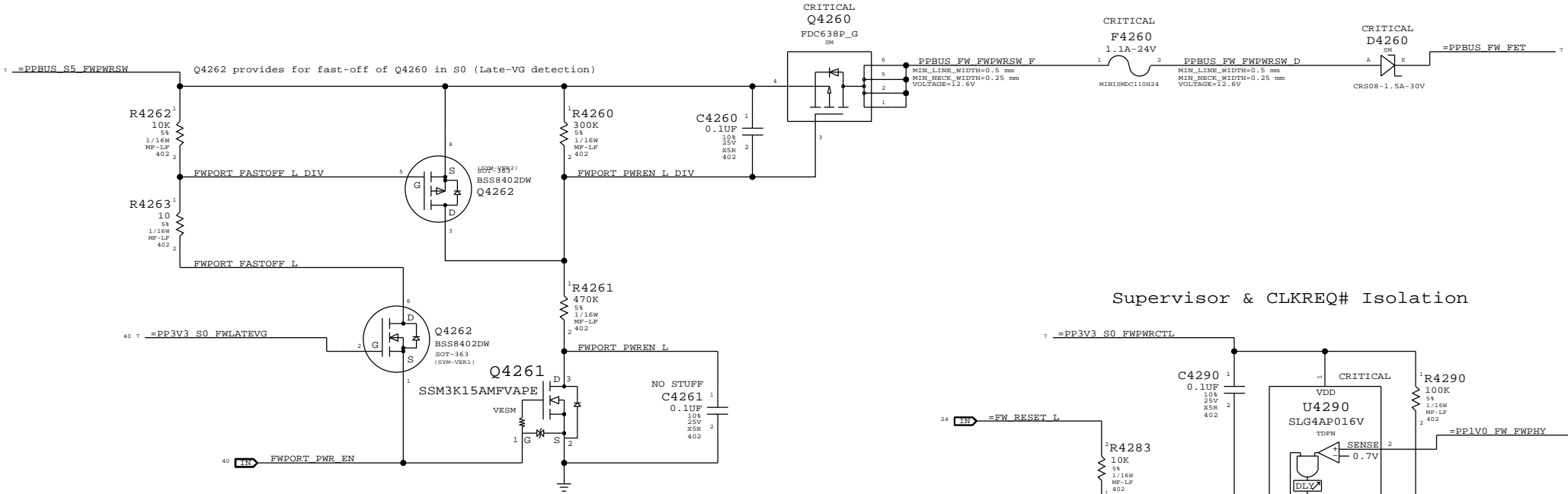
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

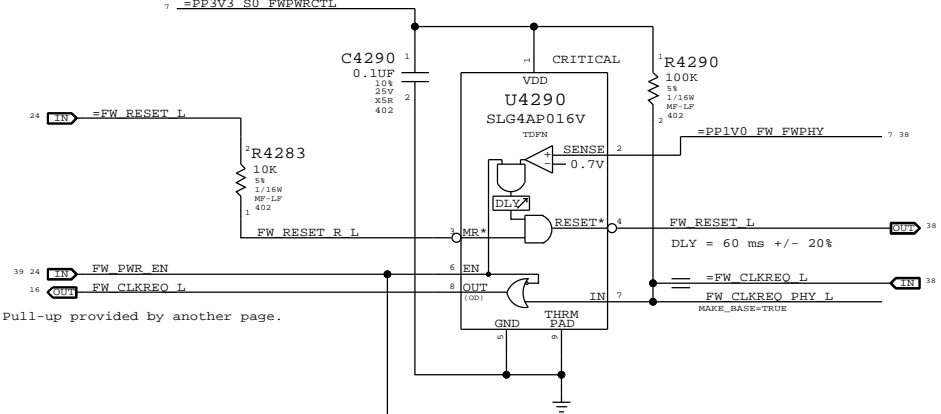
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

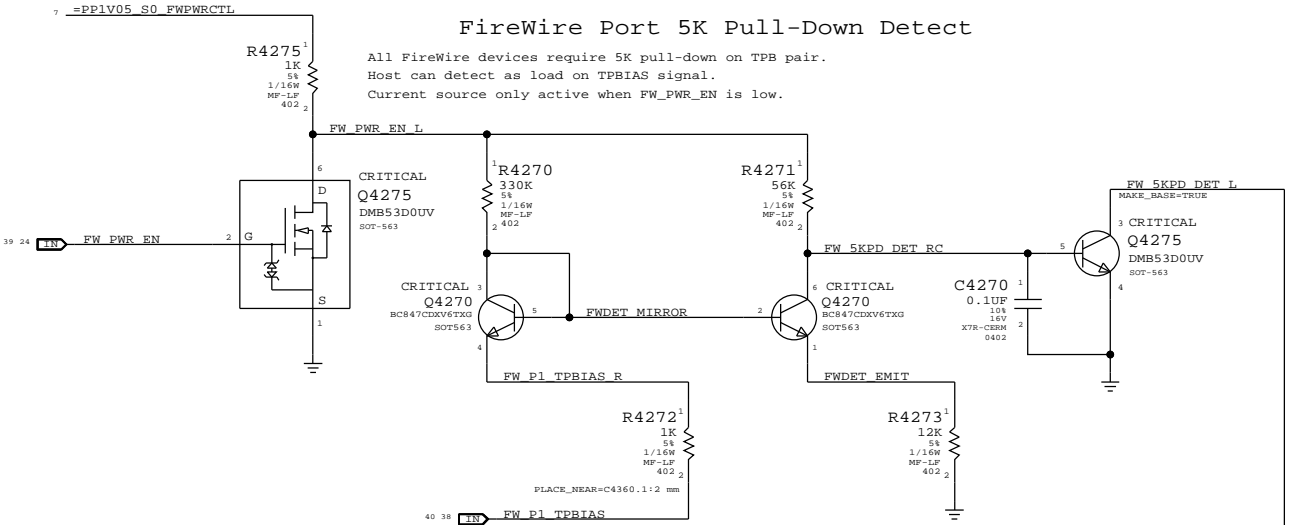


Supervisor & CLKREQ# Isolation



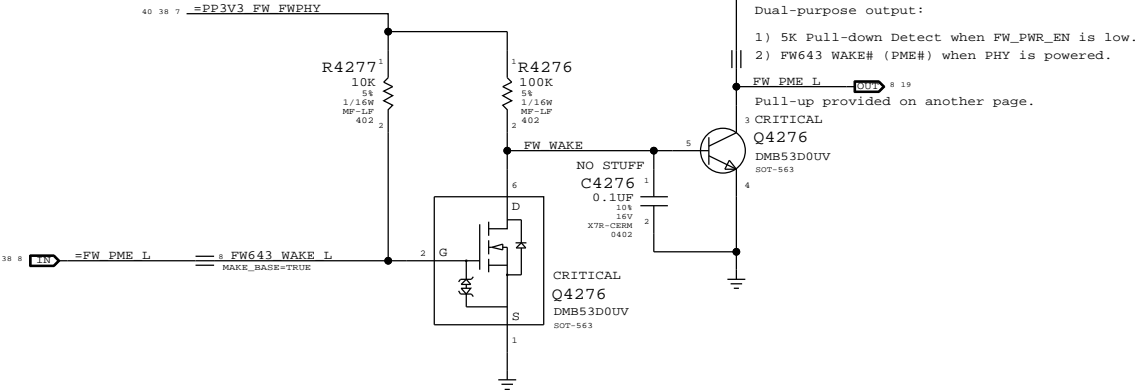
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

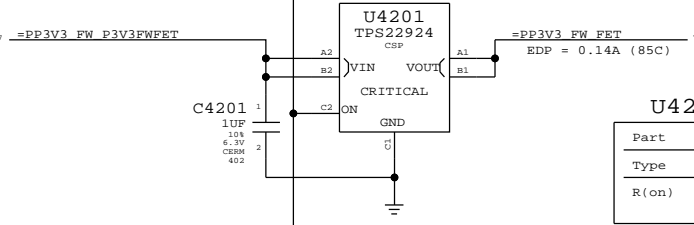
When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

3.3V FW Switch

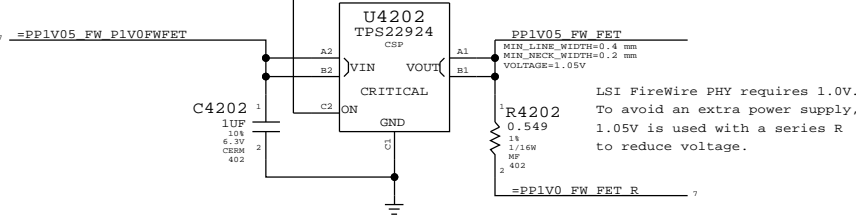


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

FireWire Port & PHY Power

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

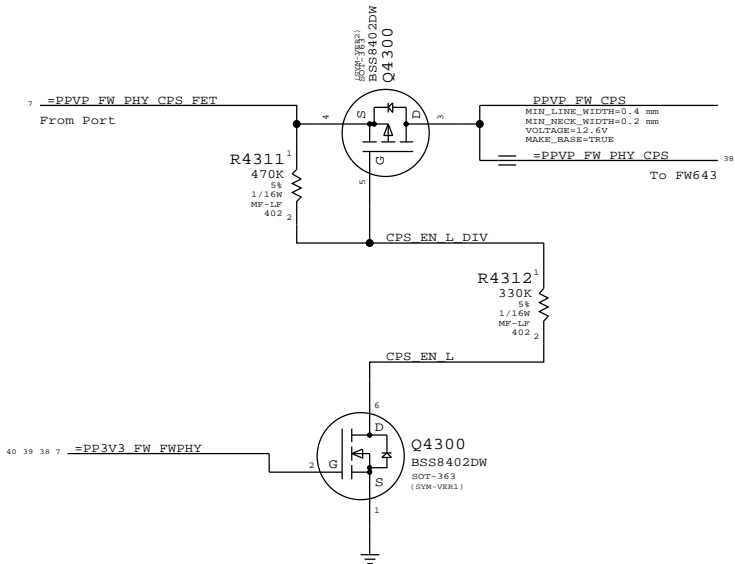
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

- (NONE)
- 1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

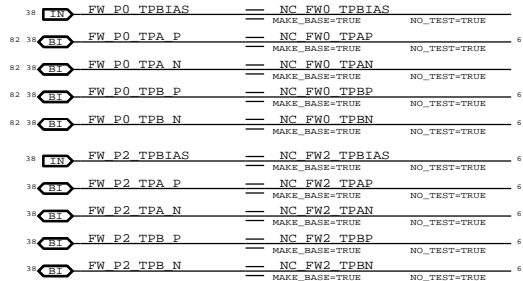
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



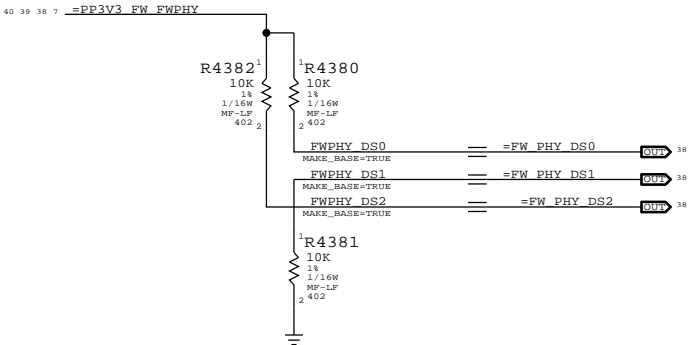
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



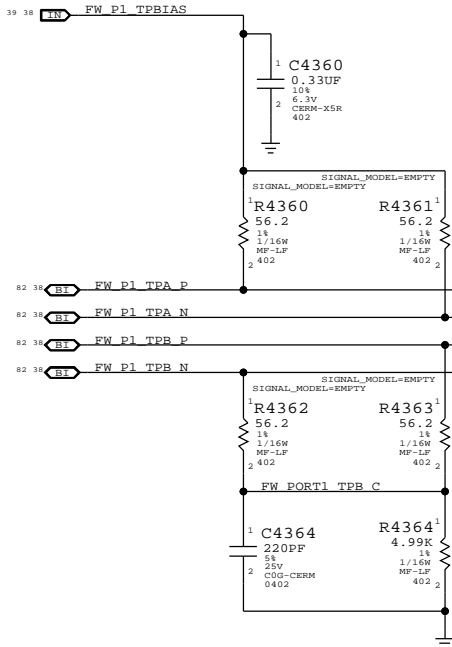
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



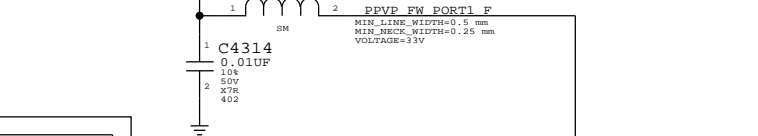
Termination

Place close to FireWire PHY

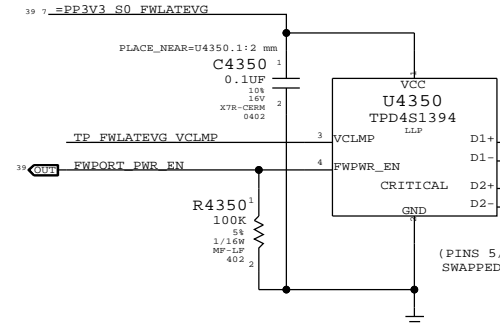


Cable Power

Note: Trace PPVP_FW_PORT1 must handle up to 5A



"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL

CRITICAL

J4310

1394B-M97

F-RT-TH

TPB(R)

TPB+

TPB-

VP

NC

VG

TPA-

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

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TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

TPA+

TPA(R)

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

FireWire Connector



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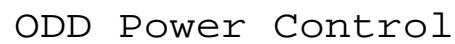
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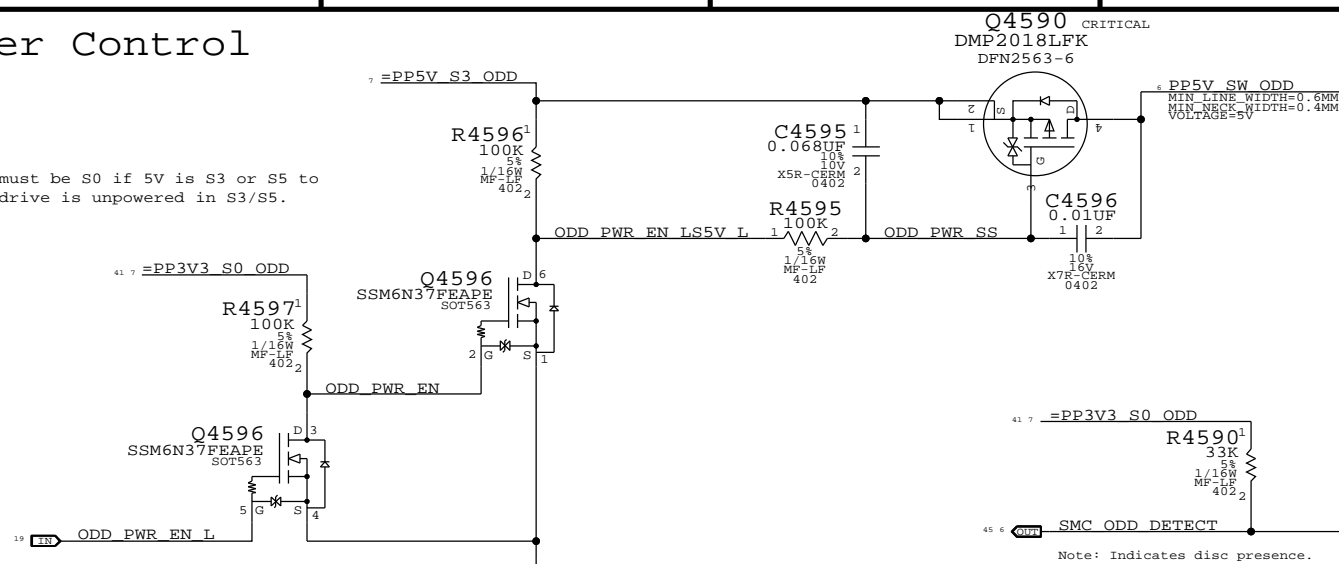
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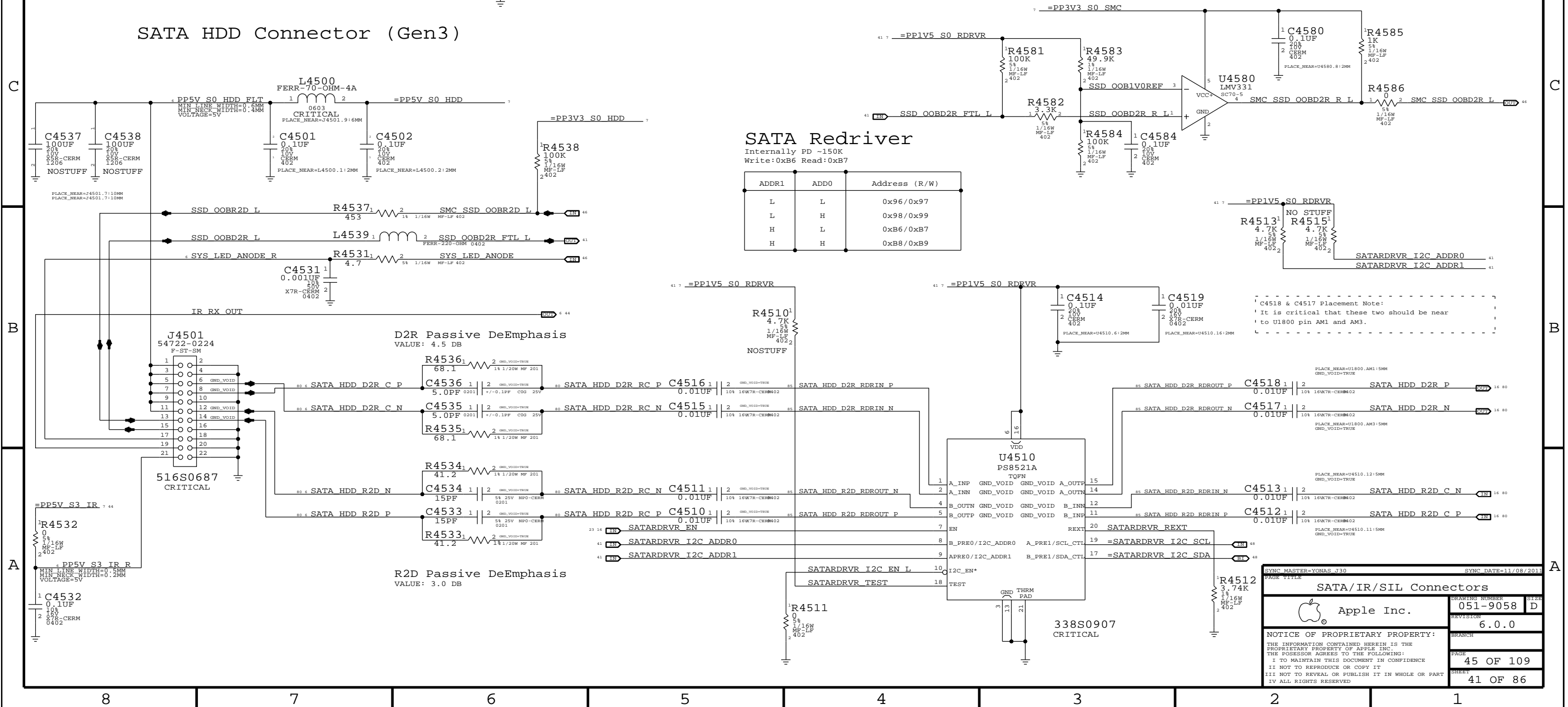
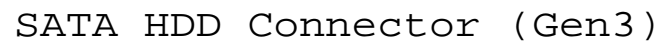


Note: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.



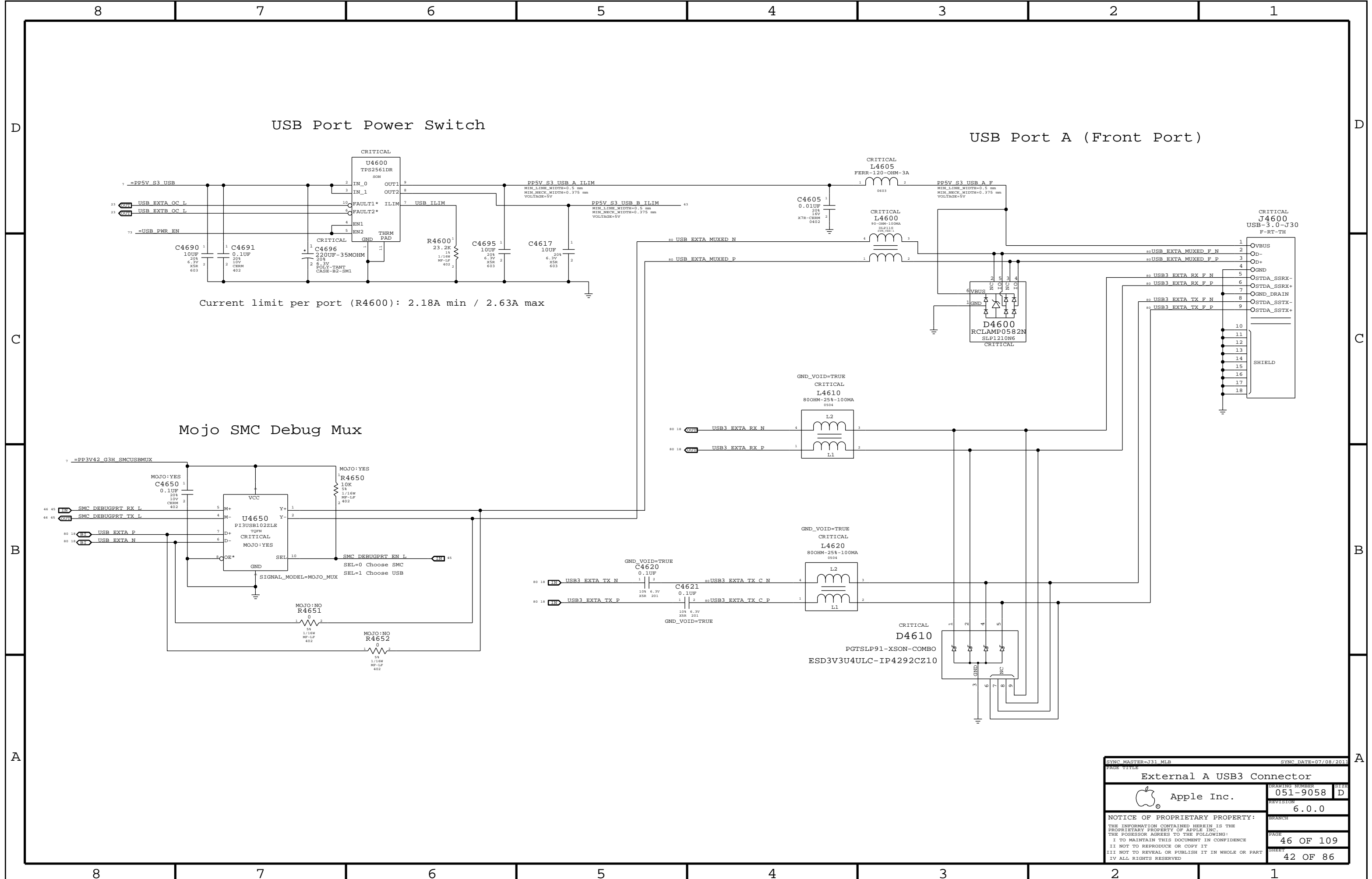
SATA OOB Comparator

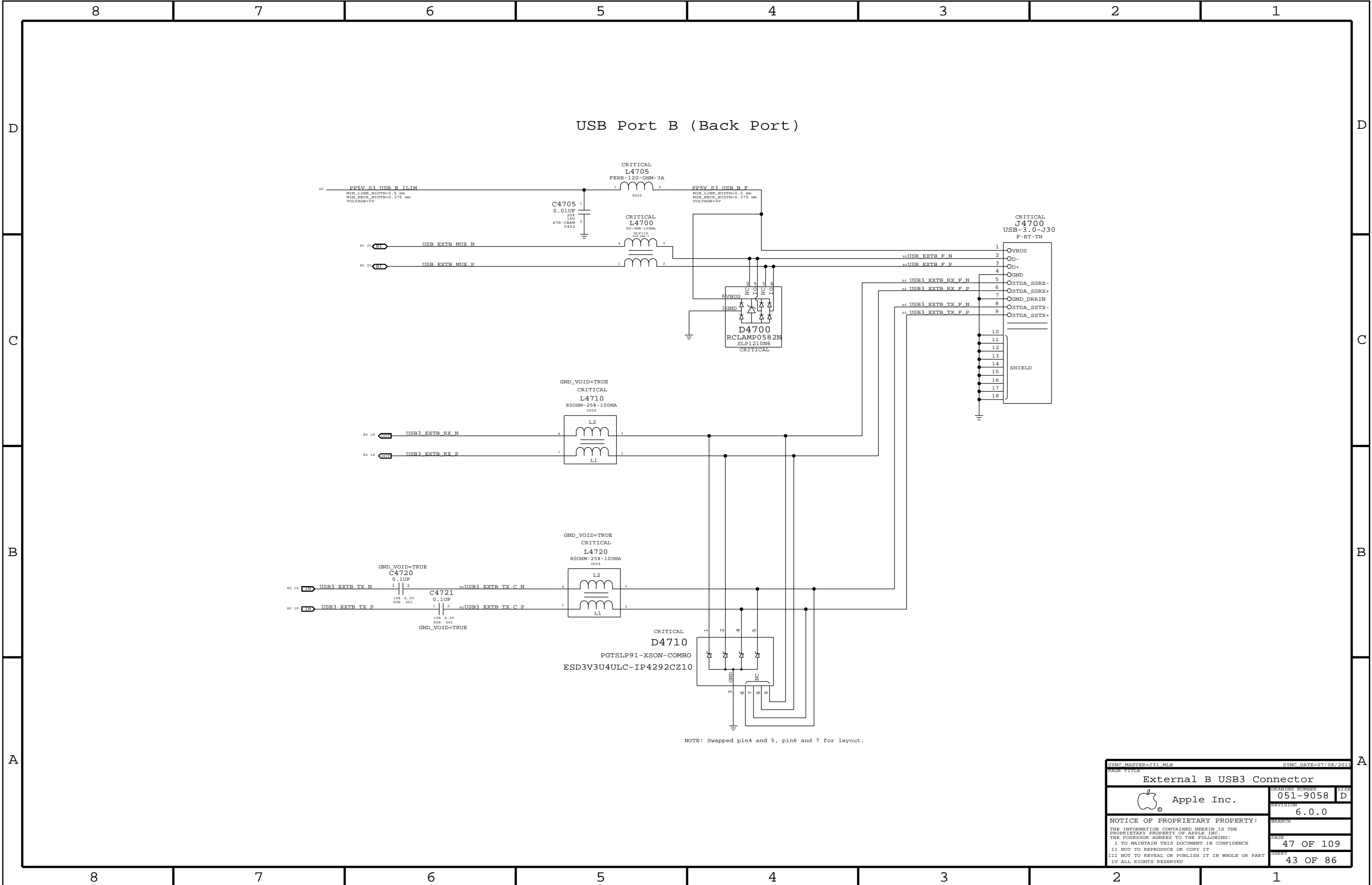
Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD




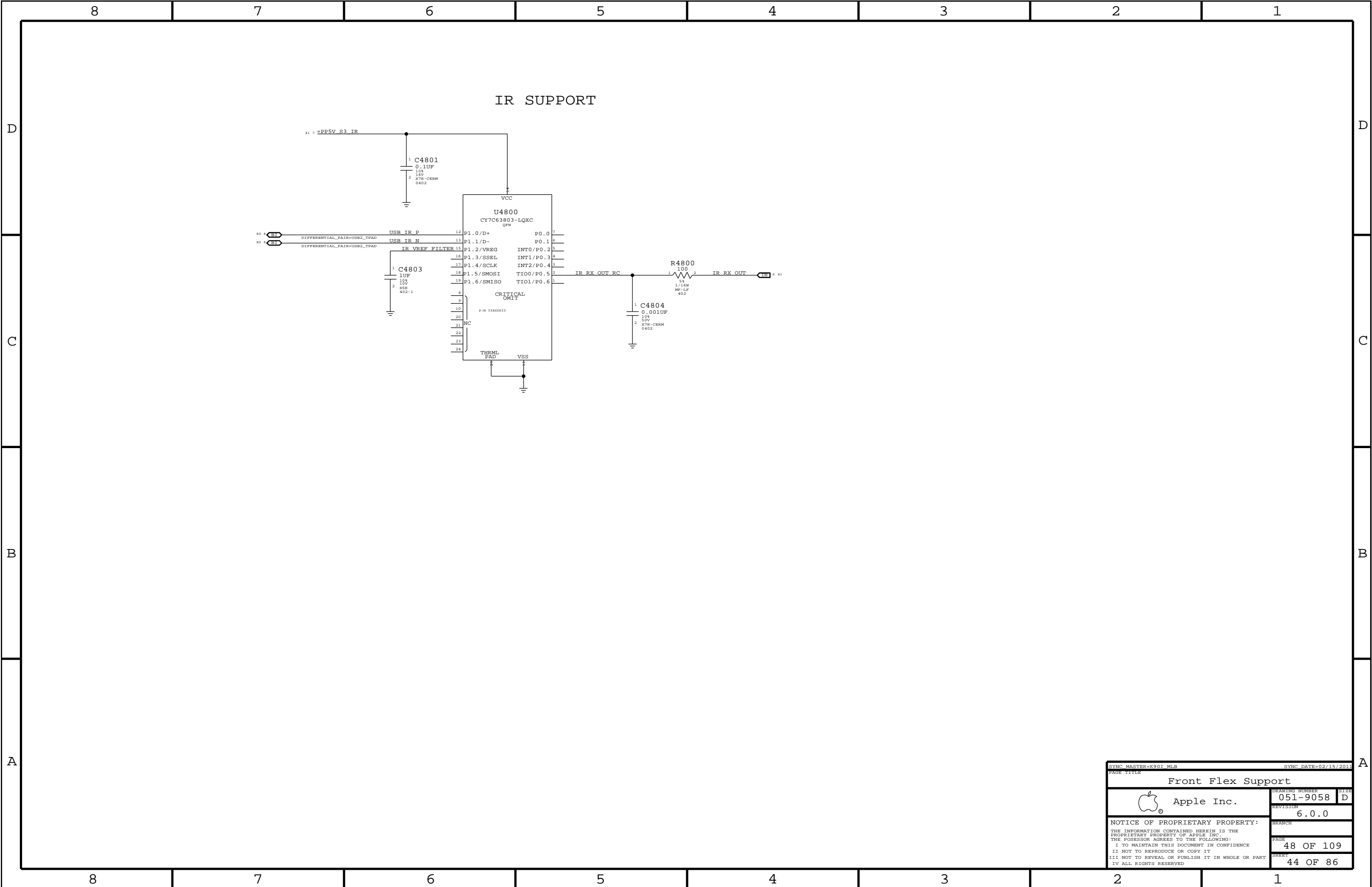
ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

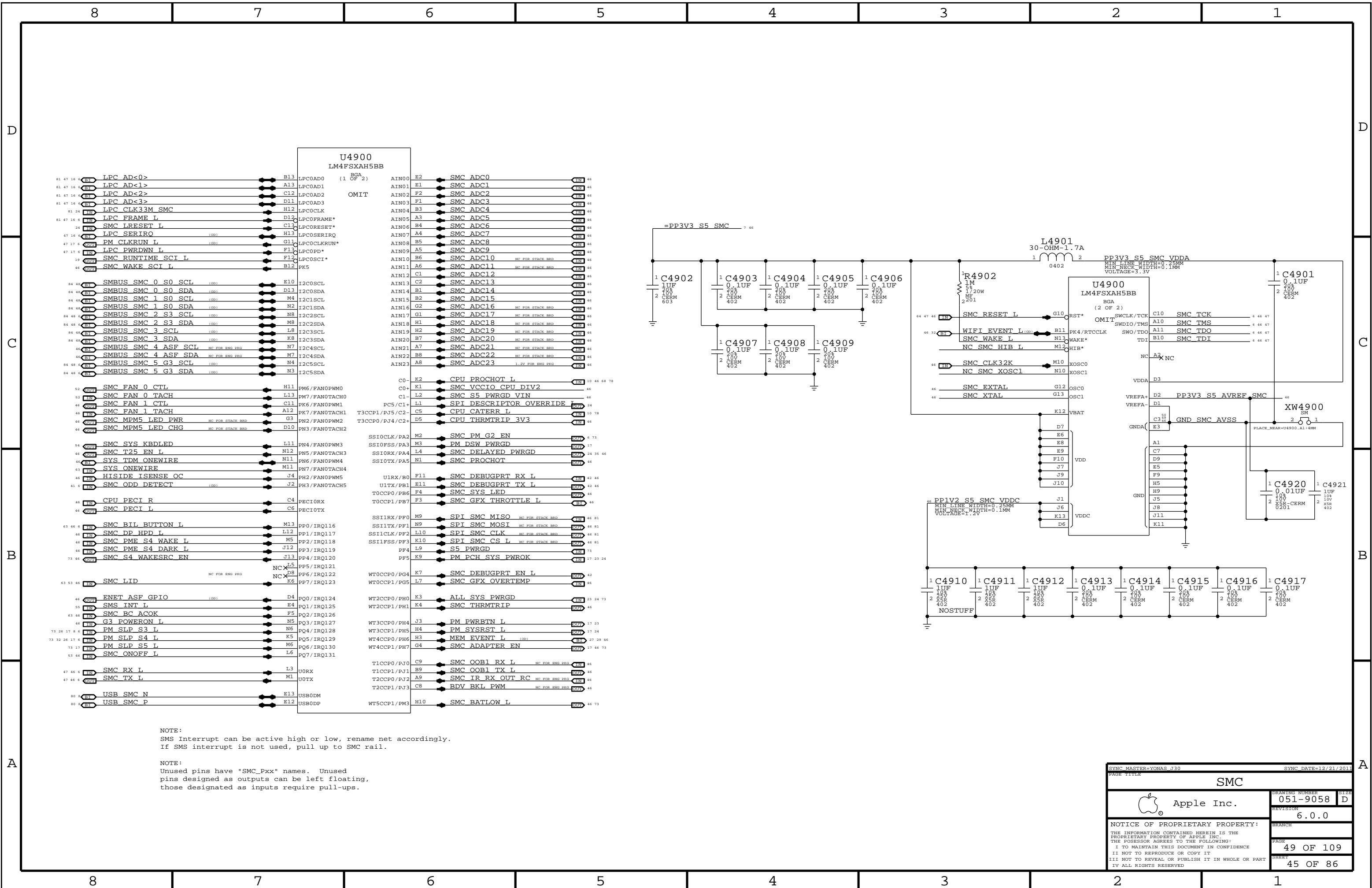
ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9





SYNC MASTER=J31 MLB		SYNC DATE=07/08/2013	
PAGE TITLE			
External B USB3 Connector			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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		BRANCH	
		PAGE	47 OF 109
		SHEET	43 OF 86

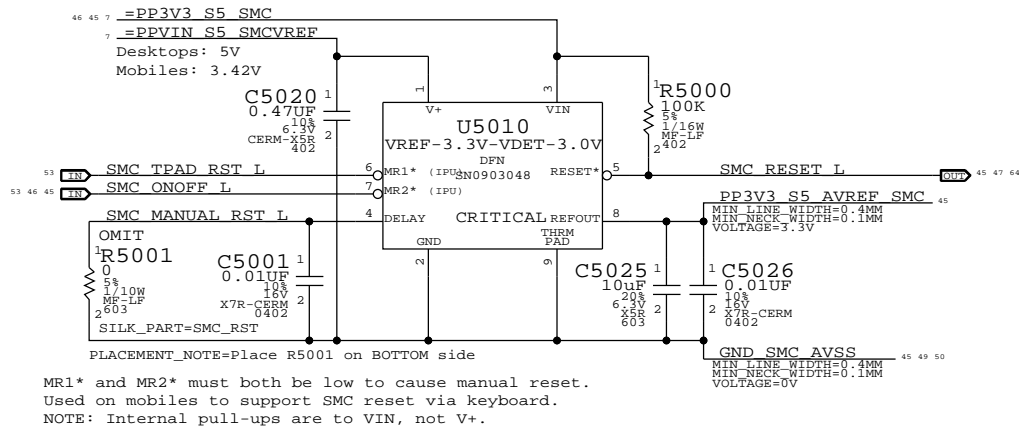




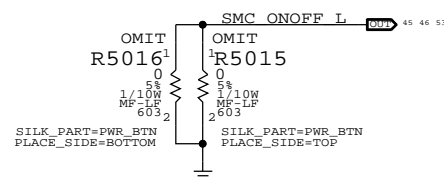
NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SMC Reset "Button", Supervisor & AVREF Supply

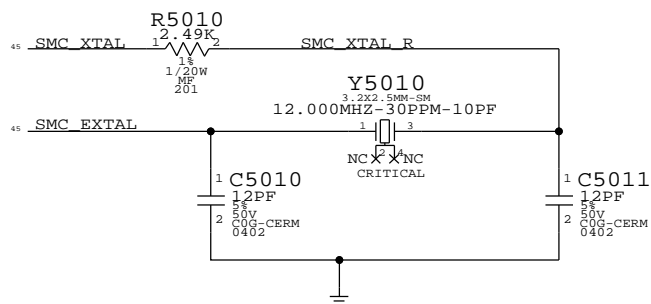


Debug Power "Buttons"



SMC Crystal Circuit

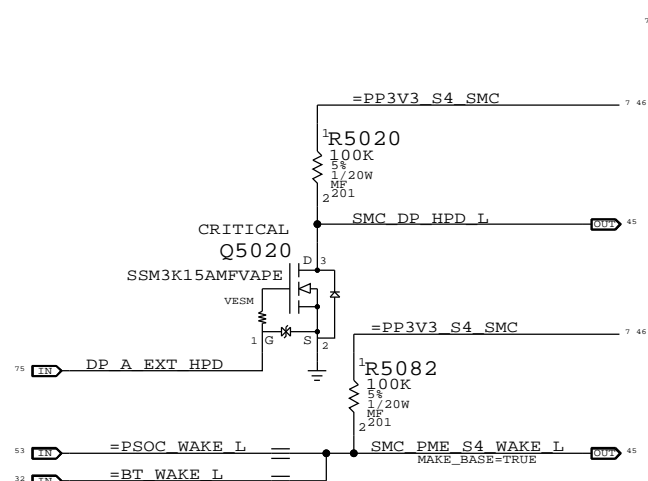
SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



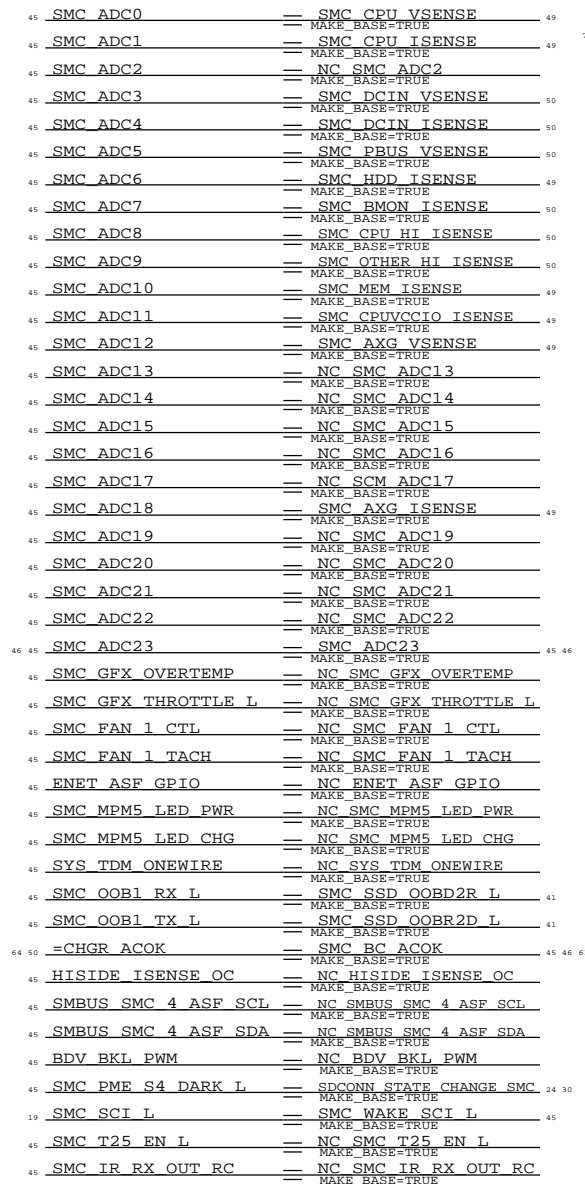
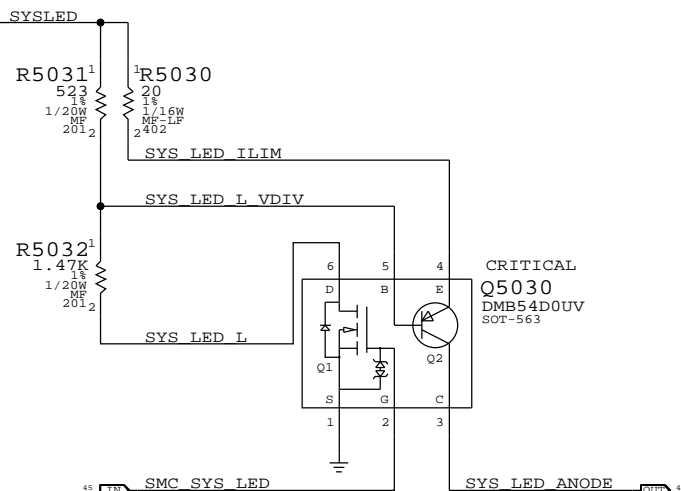
Note:
ADC10 and ADC11 are shared
with comparators on Stack Board.

Note:
Pull-up for SMC_PME_S4_DARK_L
are in page33 (R3315).

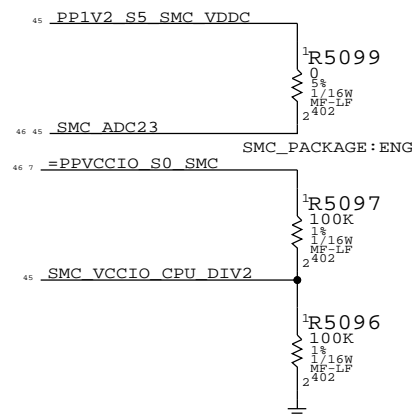
S4 HPD SMC Wake Source



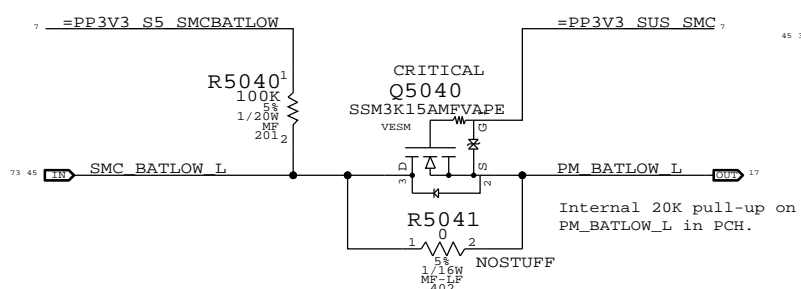
System (Sleep) LED Circuit



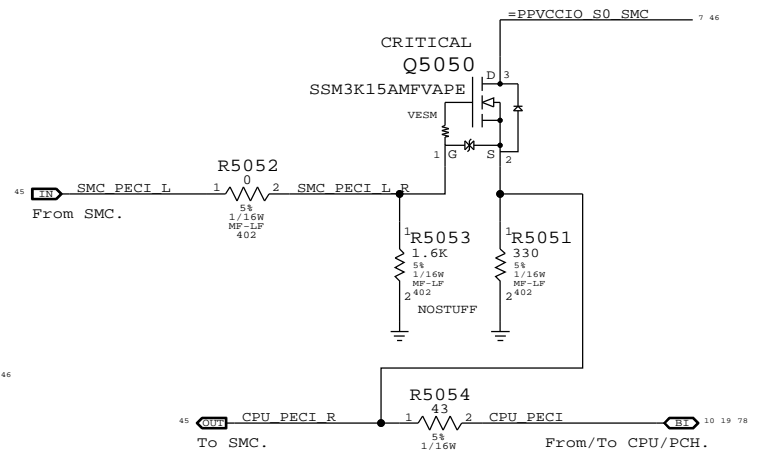
SCM12 Eng Pkg Support



BATLOW# Isolation

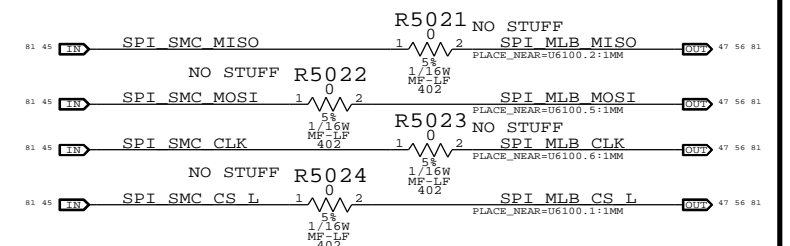


SMC12 PEFI Support

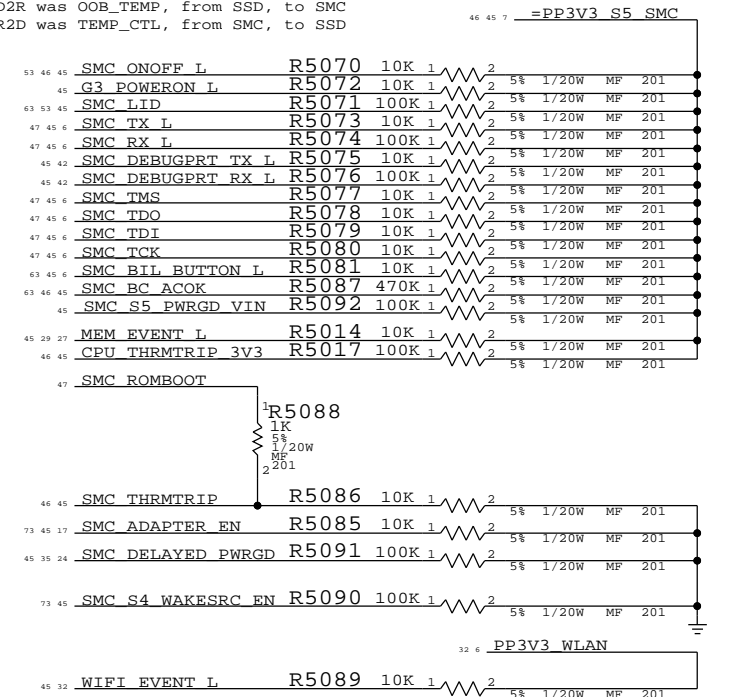



SMC12 SPI Support

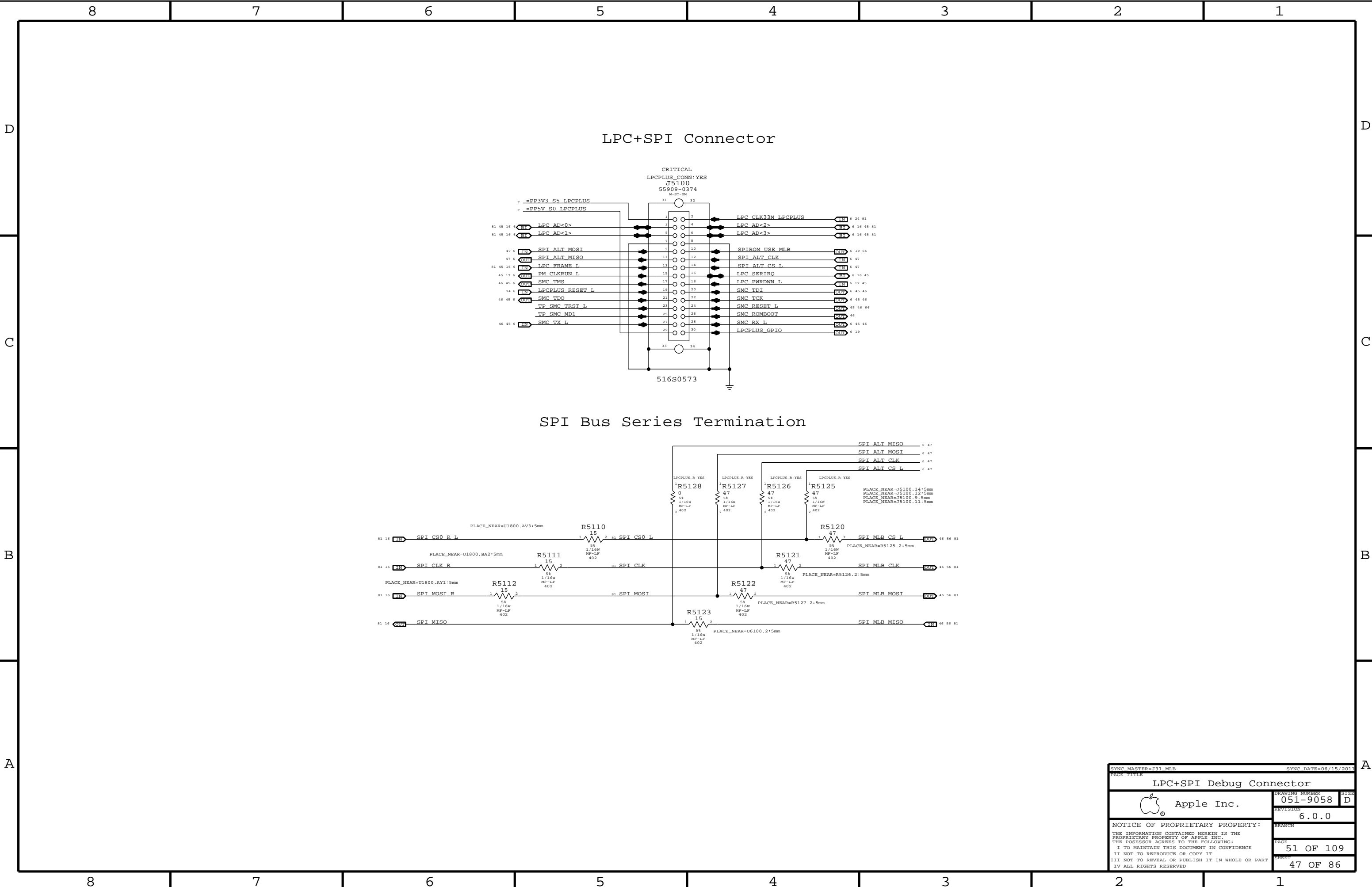
Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

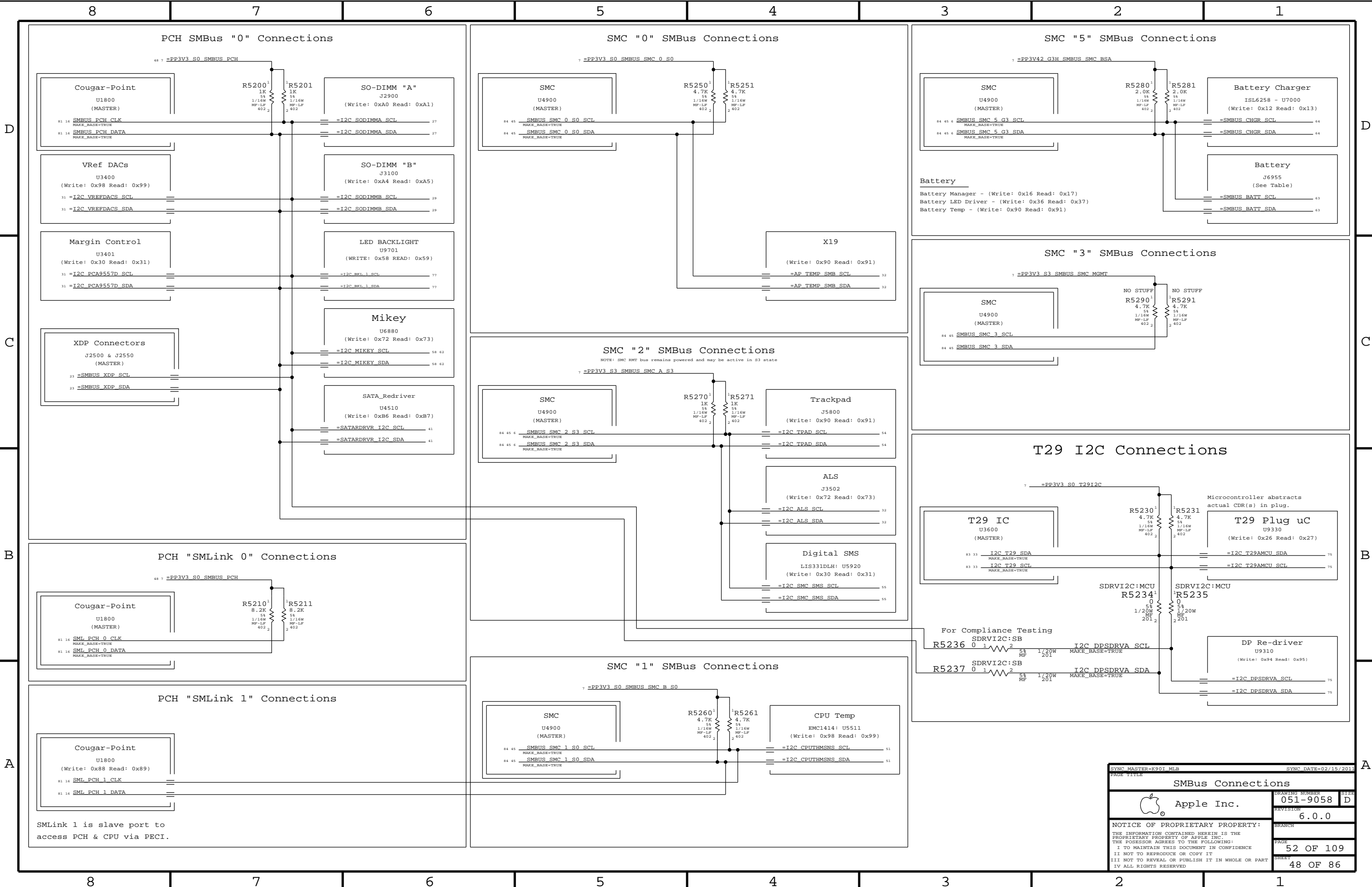


Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD



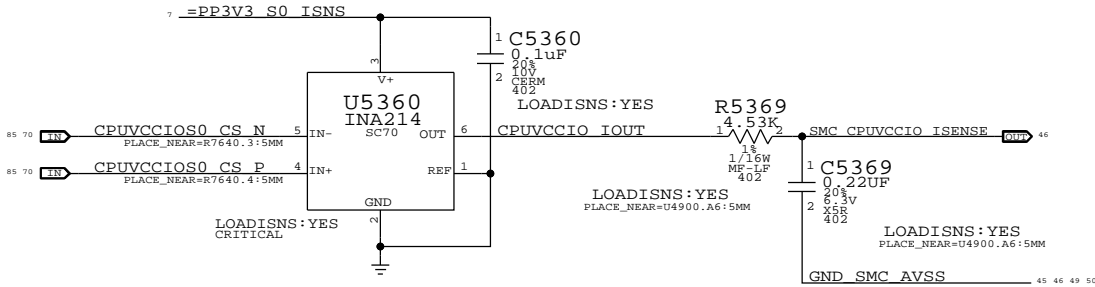
SYMC MASTER=YONAS J30		SYMC DATE=01/02/2012	
PAGE TITLE			
SMC Support			
	Apple Inc.		DRAWING NUMBER 051-9058
			SIZE D
		REVISION 6.0.0	
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		SHEET 46 OF 86	





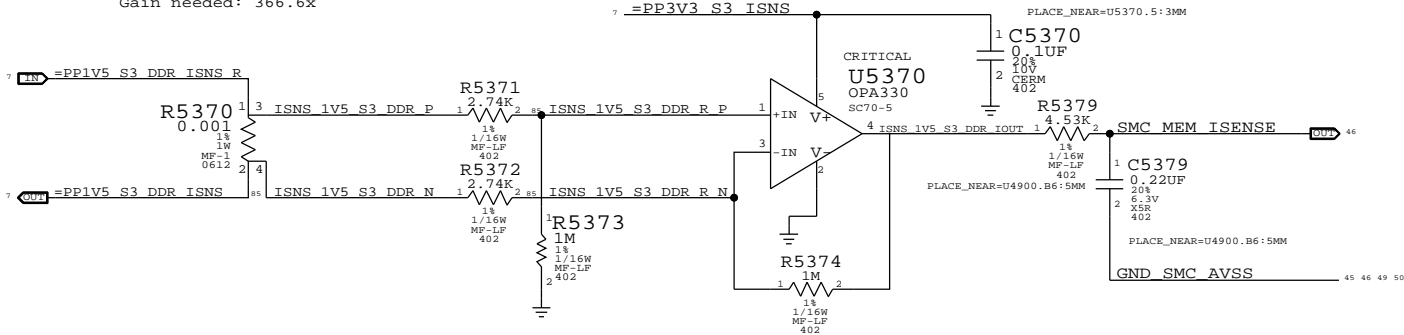
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 100x, EDP: 20.1 A
Rsense: 0.001 (R7640)
V across Rsense: 20.1 mV
Gain needed: 164.2x



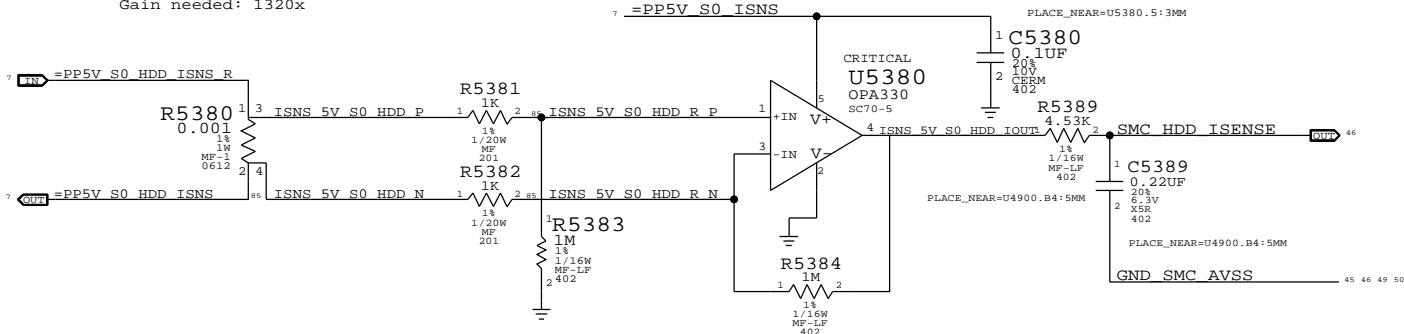
DDR 1.5V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 366.6x

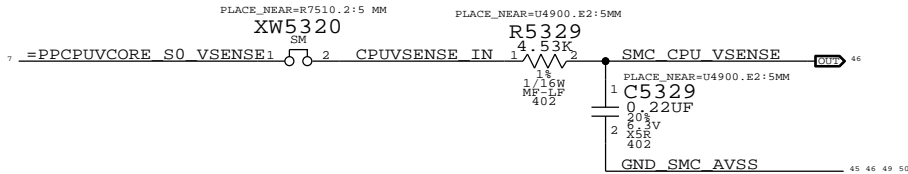


HDD Current Sense (IHDC)

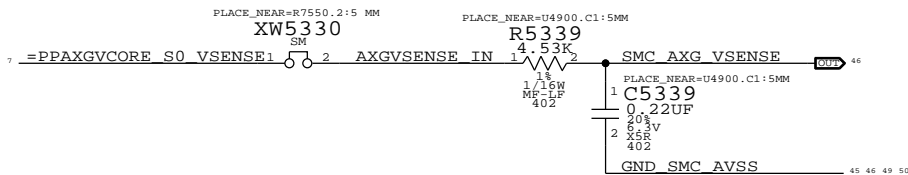
Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R5380)
V across Rsense: 2.5 mV
Gain needed: 1320x



CPU Core Voltage Sense (VC0C)

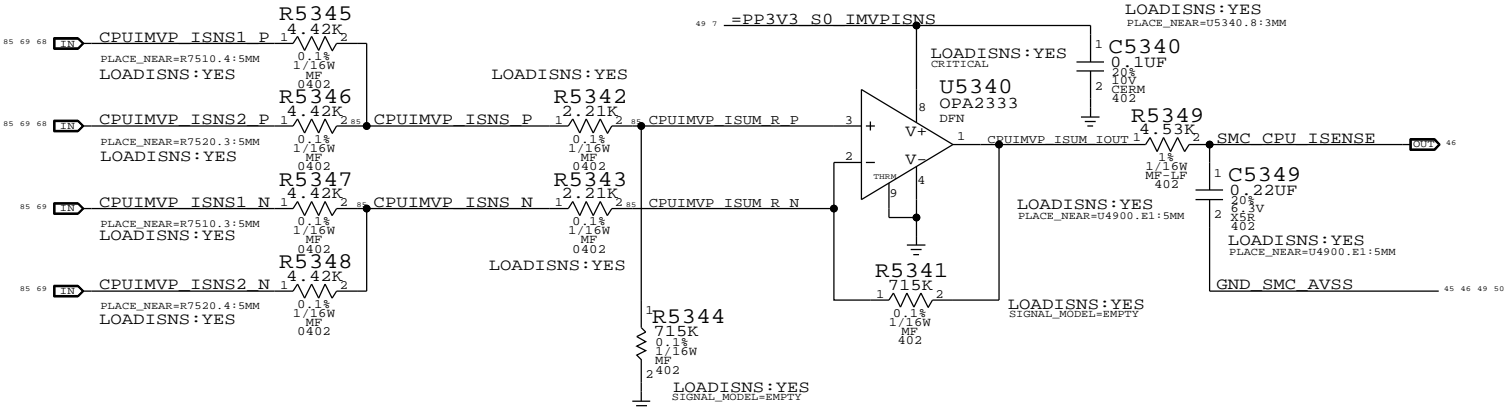


AXG Core Voltage Sense (VN0C)



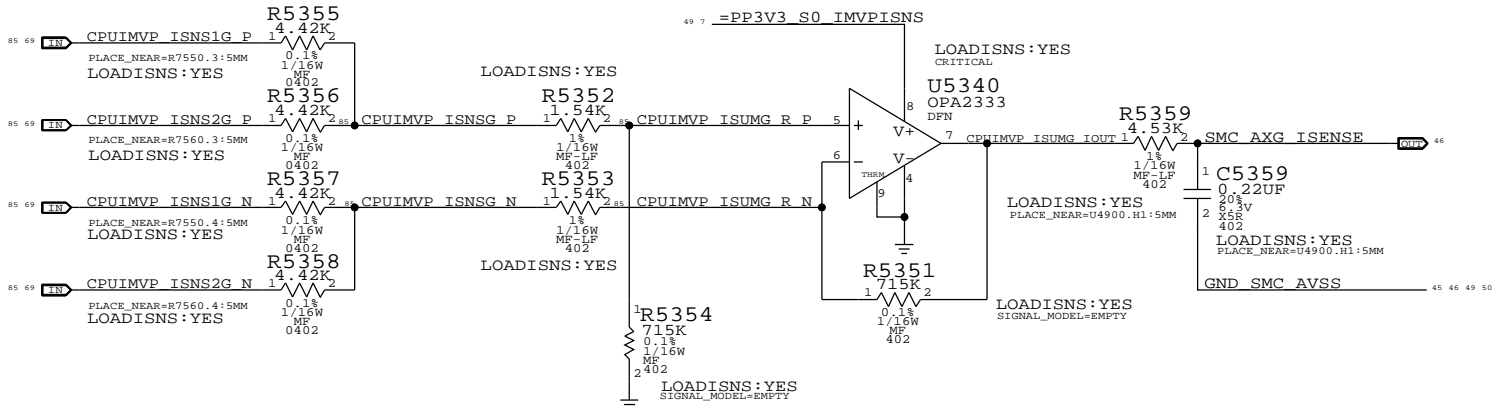
CPU Core Load Side Current Sense (IC0C)

Gain: 161.5x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
Gain needed: 166.1x




AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
Gain needed: 191.3x

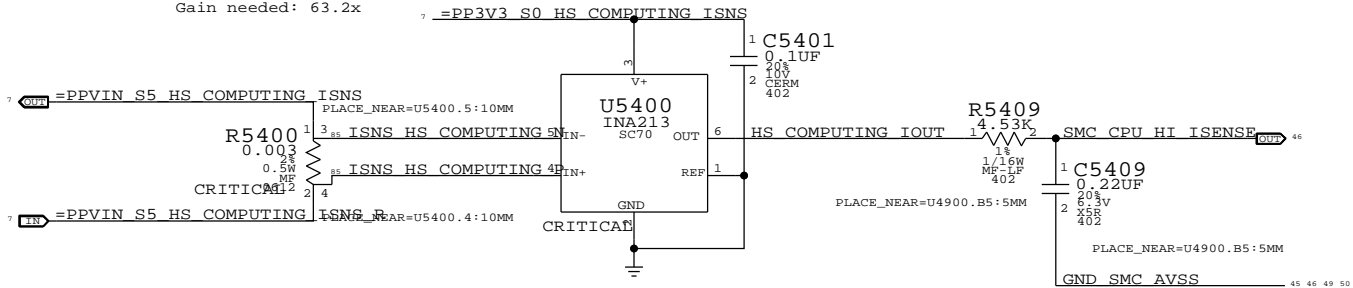


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	3	RES,MTL,FLIM,100K,1/16W,0402,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=LINDA J30		SYNC DATE=09/28/2011	
PAGE TITLE			
Power Sensors: Load Side			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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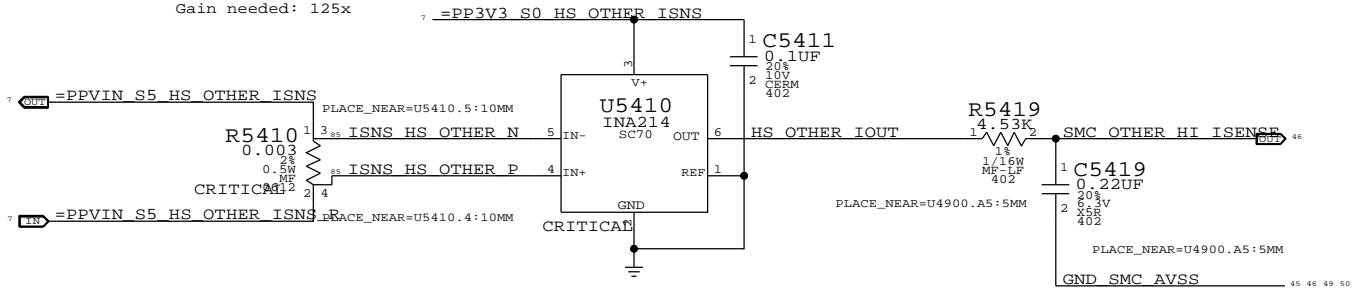
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
Gain needed: 63.2x



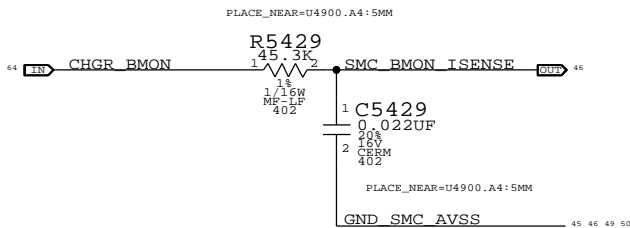
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
Gain needed: 125x



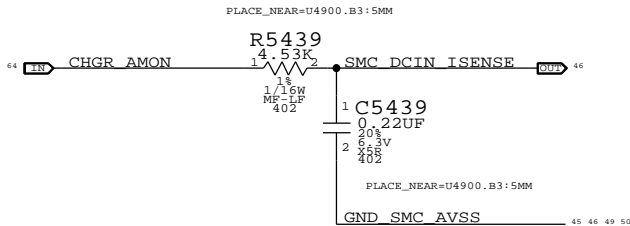
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Current Measured: 9.2 A

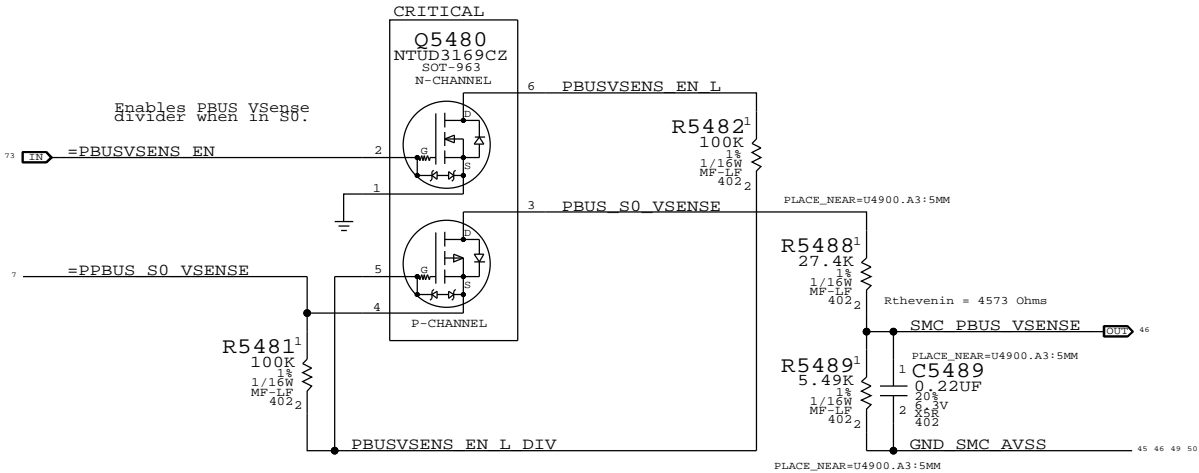


DC-In (AMON) Current Sense (ID0R)

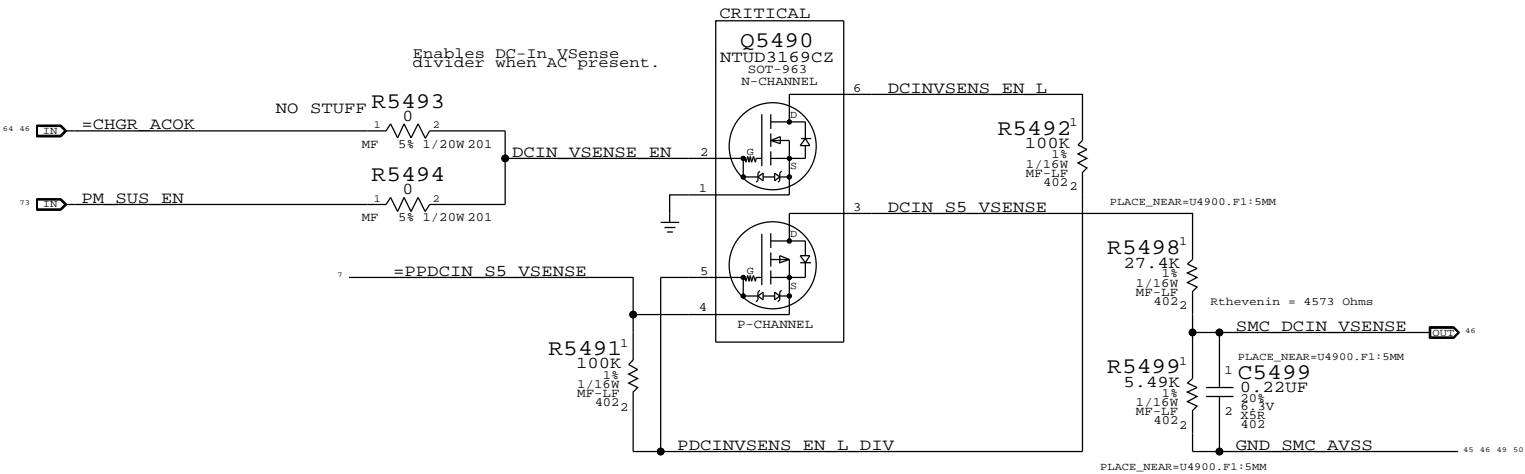
Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Current Measured: 8.3 A



PBUS Voltage Sense & Enable (VP0R)

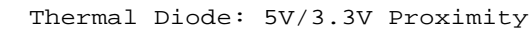


DC In Voltage Sense & Enable (VD0R)



SYNC MASTER=YONAS_J30		SYNC DATE=11/03/2011	
PAGE TITLE		Power Sensors: High Side	
DRAWING NUMBER		051-9058	SIZE D
REVISION		6.0.0	BRANCH
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```
I2C Write, 0x98, I2C Read: 0x99
```



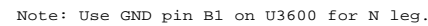
Thermal Diode: Memory Proximity


Thermal Sensor: CPU Proximity

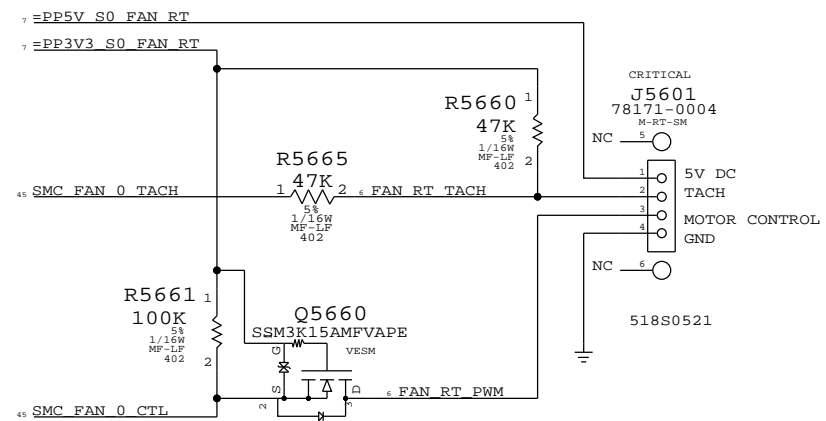
```


' Placement Note:
' Place U5511 on bottom side under CPU
'

```

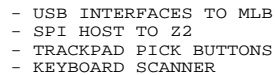


SYNC MASTER=YONAS J30		SYNC DATE=08/01/2011	
PAGE TITLE			
Thermal Sensors			
		DRAWING NUMBER 051-9058	
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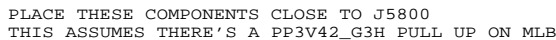


SYNC MASTER-K90I MLE		SYNC DATE=02/15/2018	
PAGE TITLE			
Fan		DRAWING NUMBER 051-9058	SIZE D
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- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB



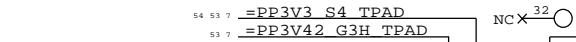
```

THE TPAD BUTTONS WILL BE DISABLED
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

```

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A 800A	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD	60mA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60mA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8mA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14mA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4mA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

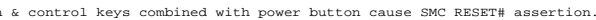
54 53 7 =PP3V3 S4 TPAD
53 7 =PP3V42 G3H TPAD



and control keys combined with power button cause SMC RESET# assertion.

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



D

C

B

A

D

C

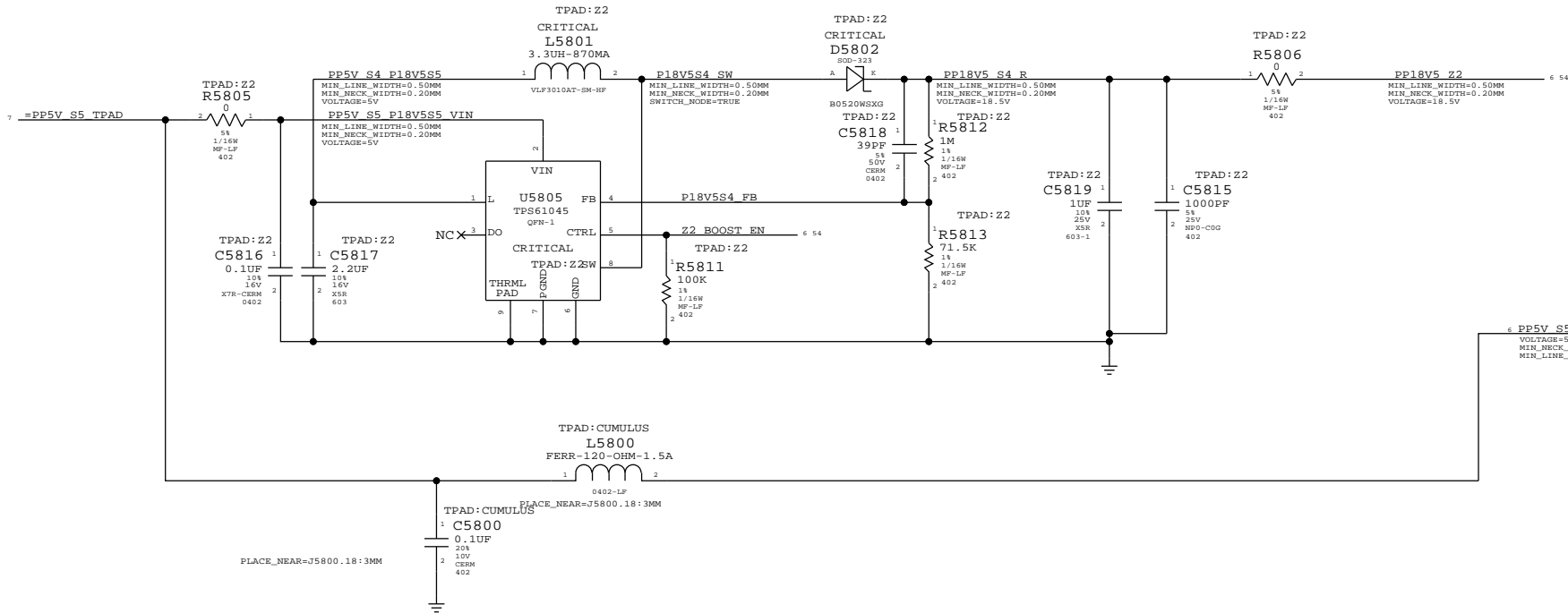
B

A

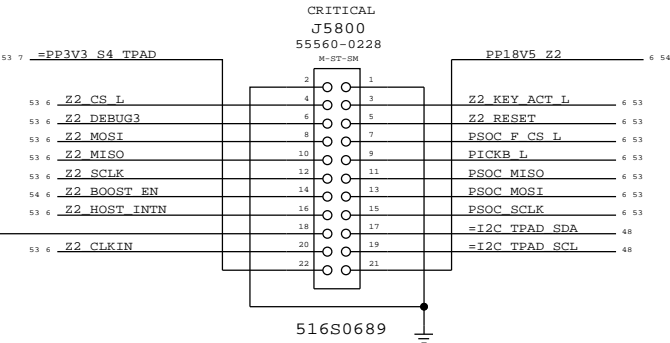
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:

- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

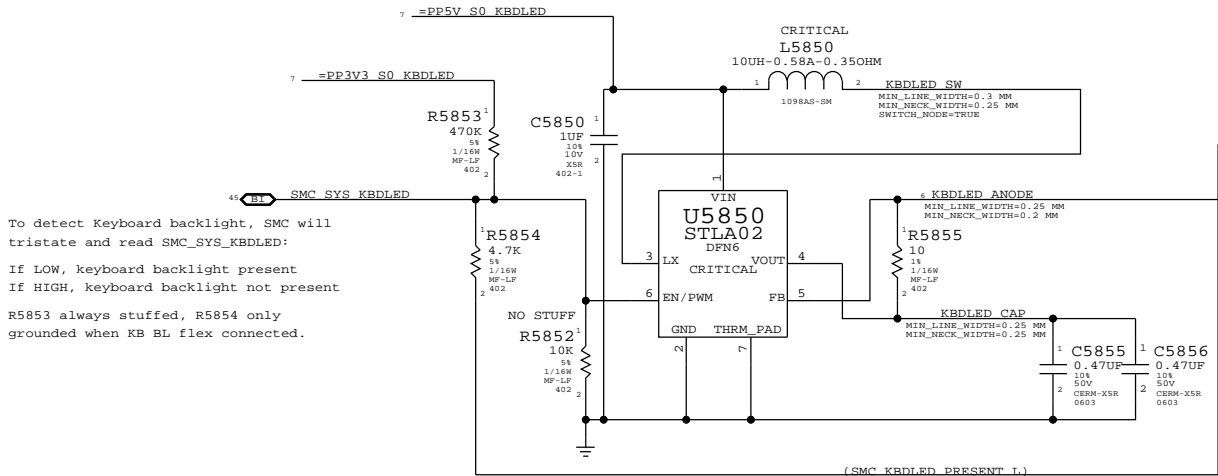


IPD Flex Connector

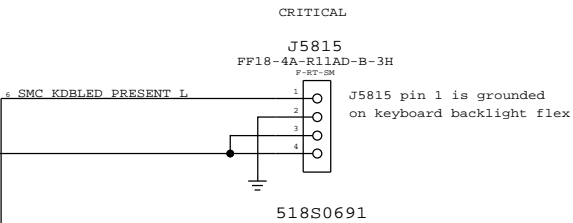


PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

Keyboard Backlight Driver & Detection

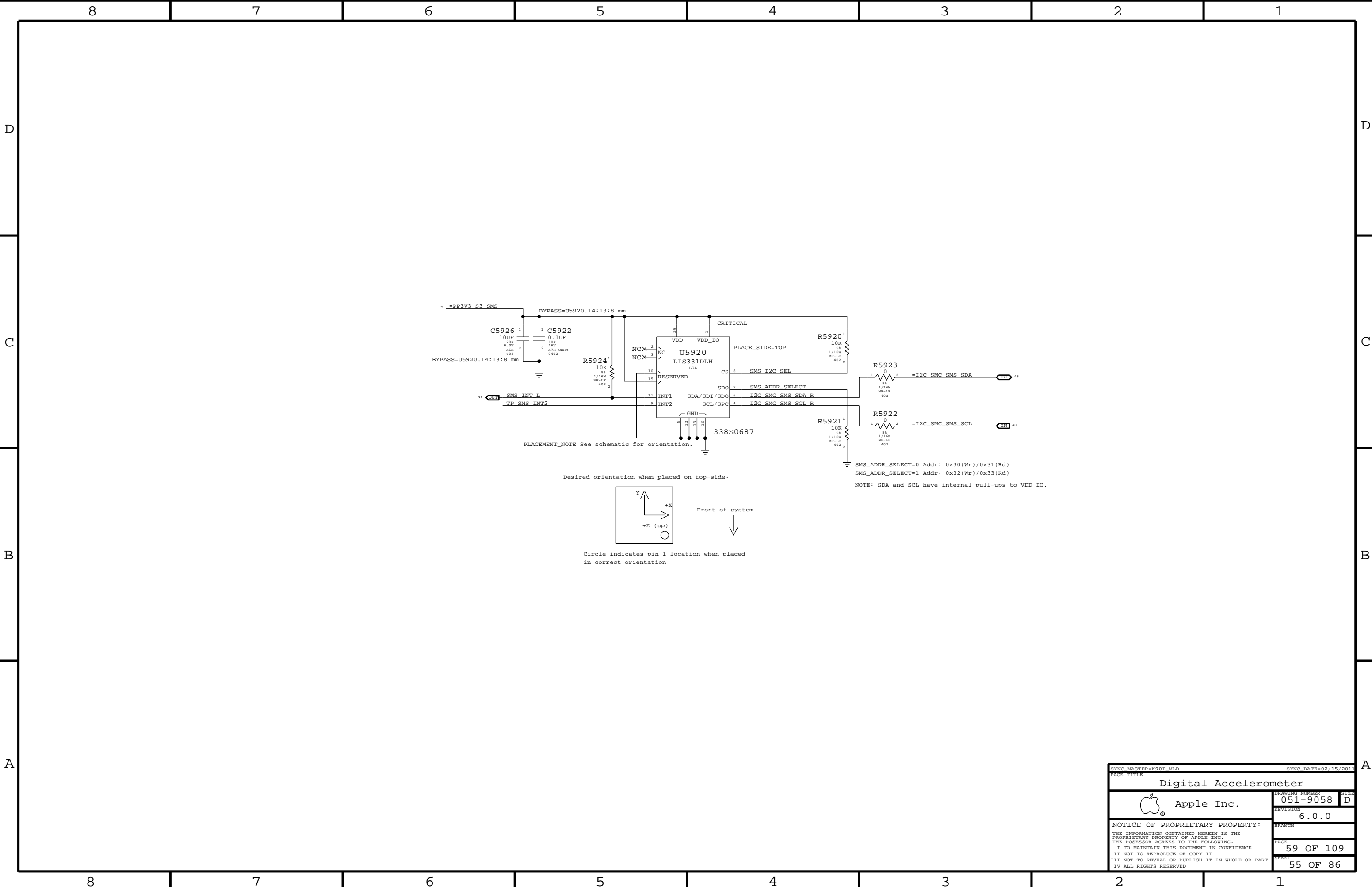


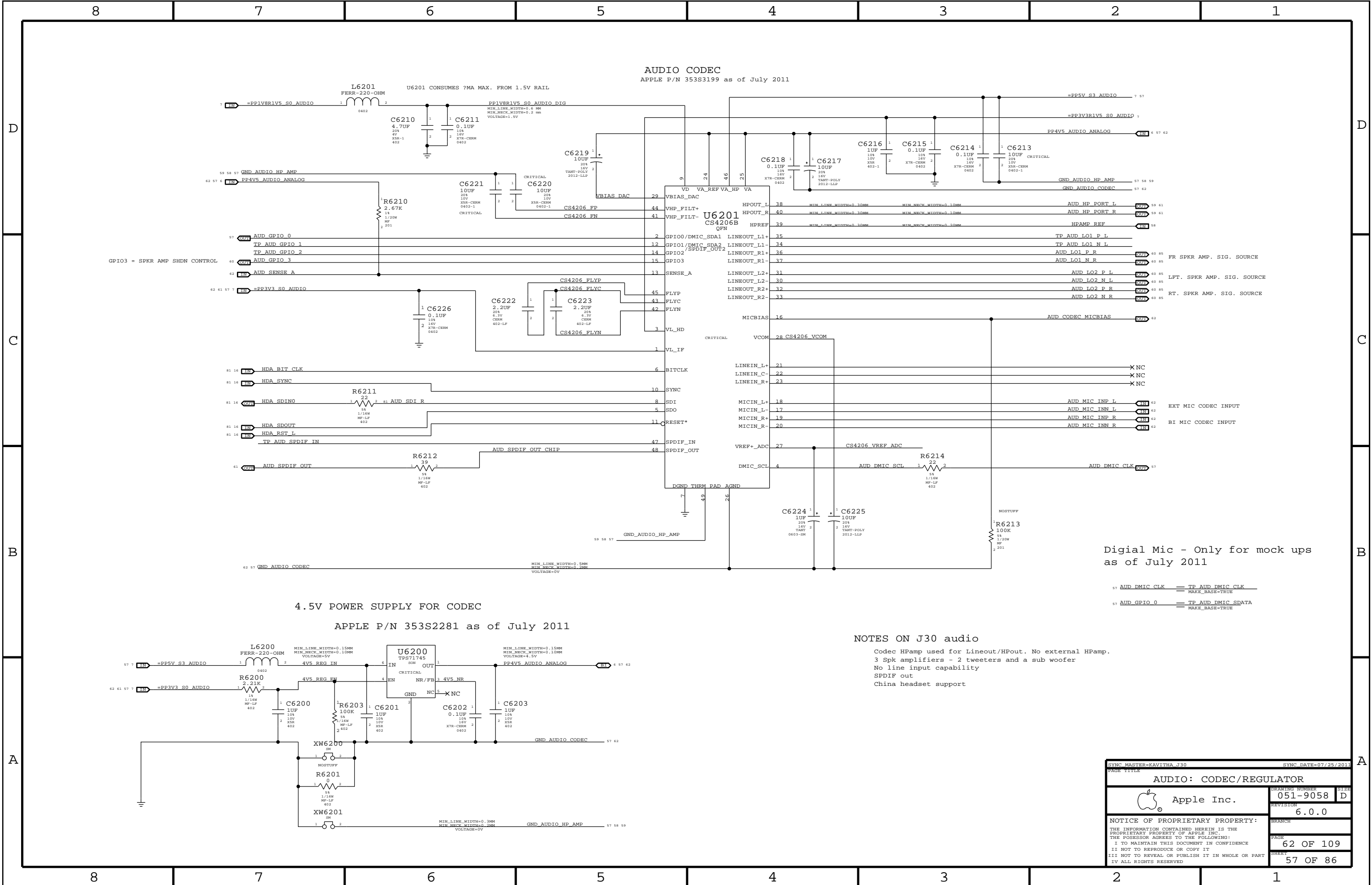
Keyboard Backlight Connector




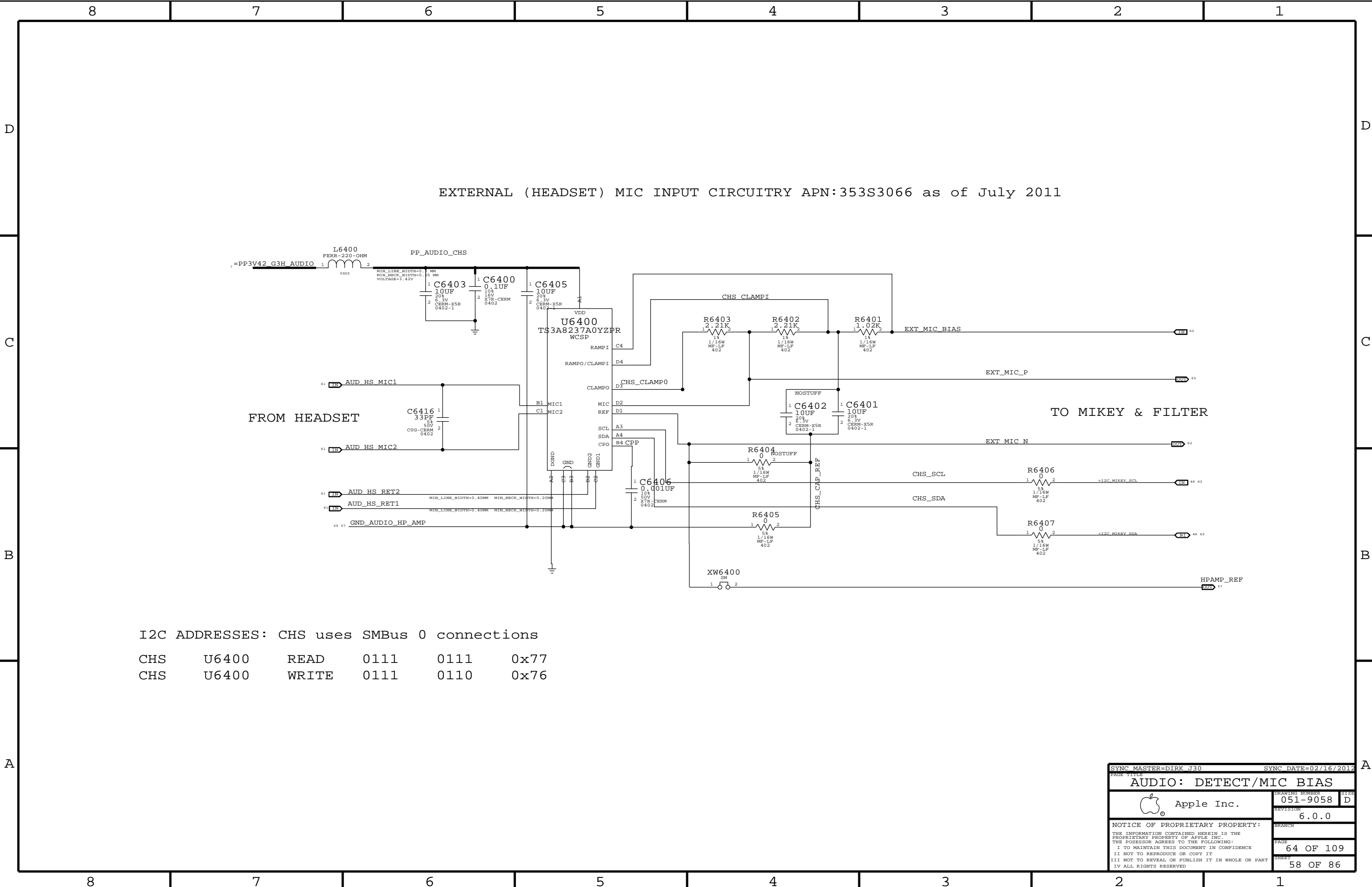
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

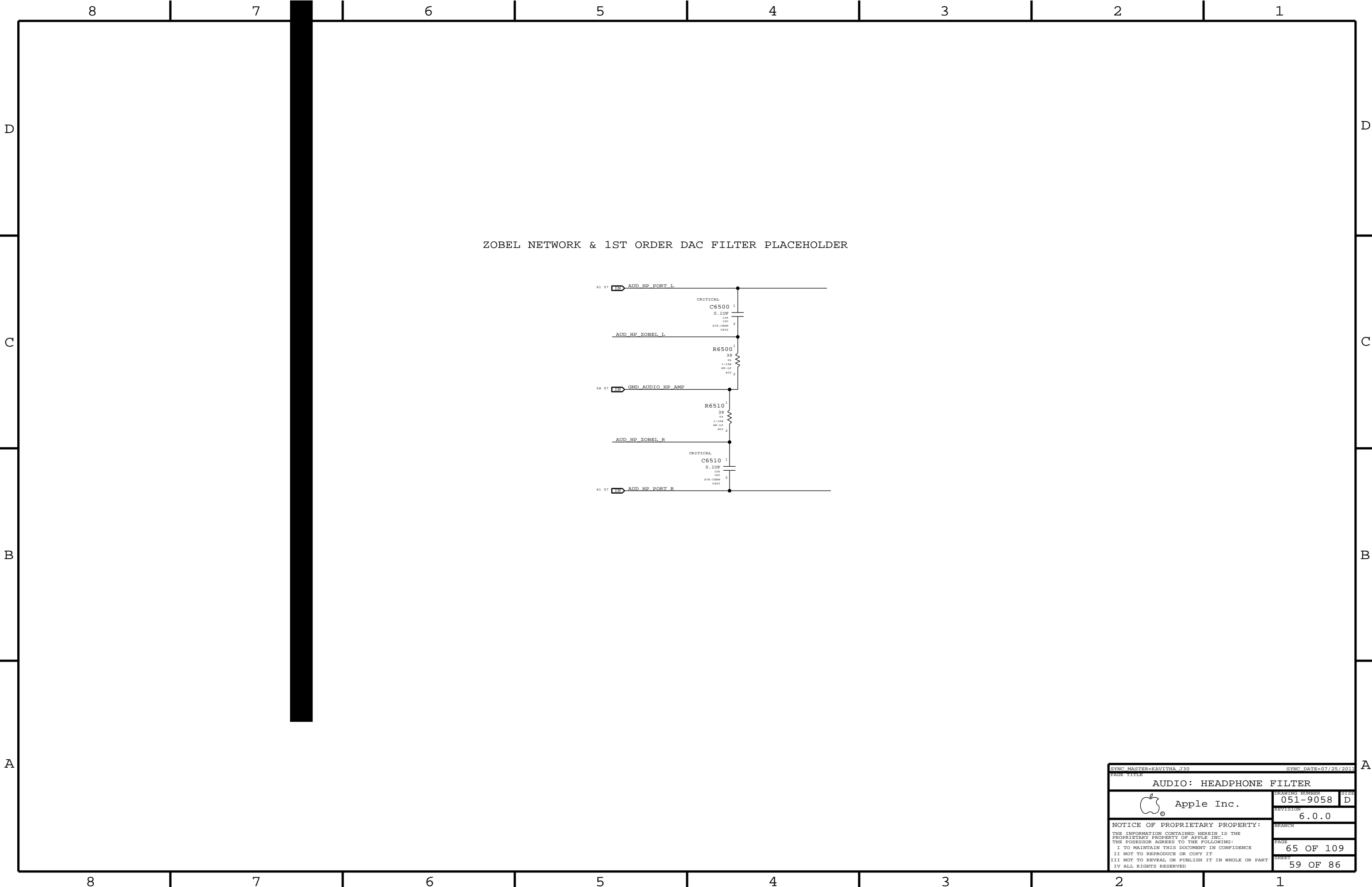
WELLSPRING 2		DRAWING NUMBER		SIZE
Apple Inc.		051-9058		D
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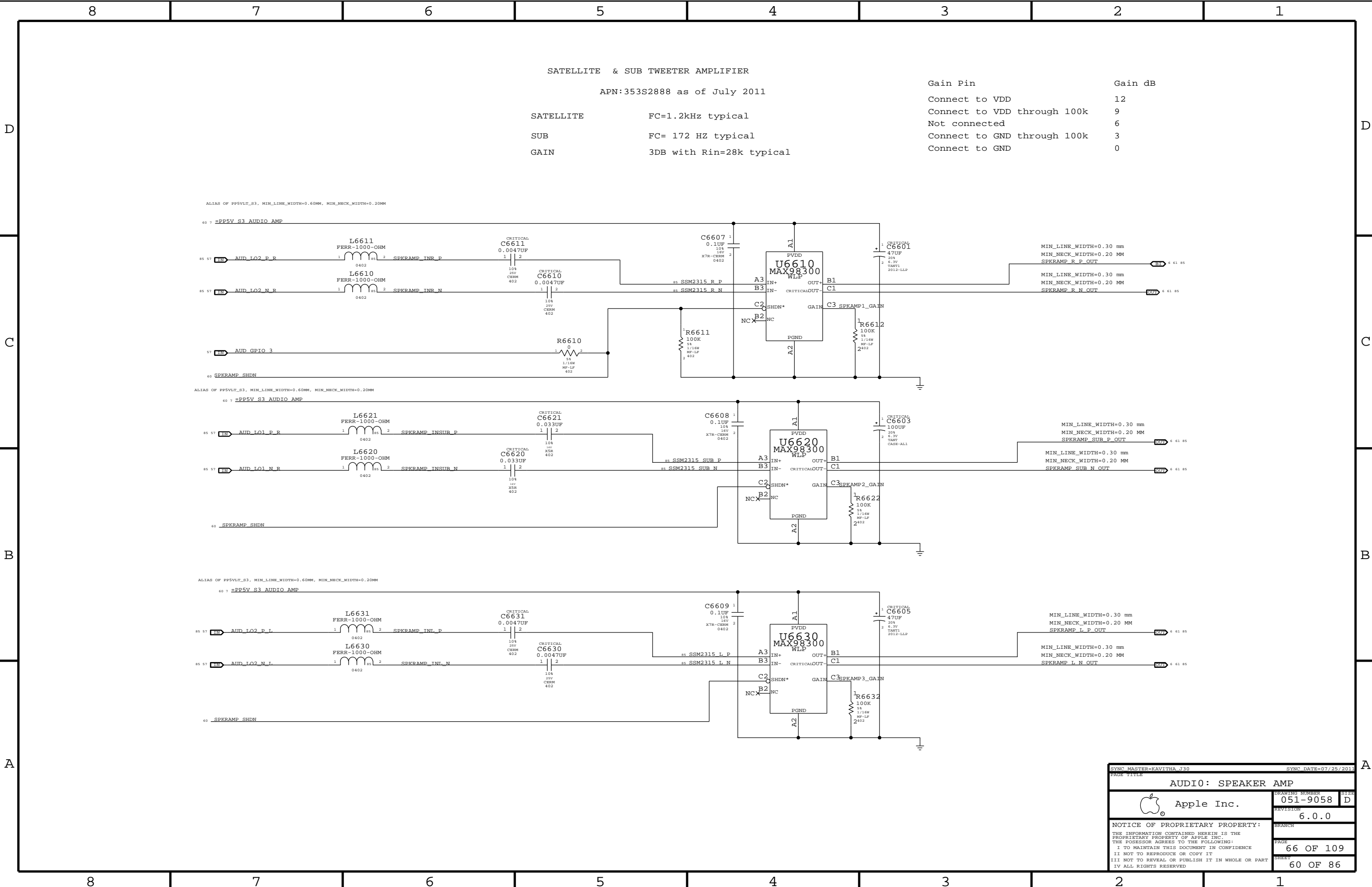


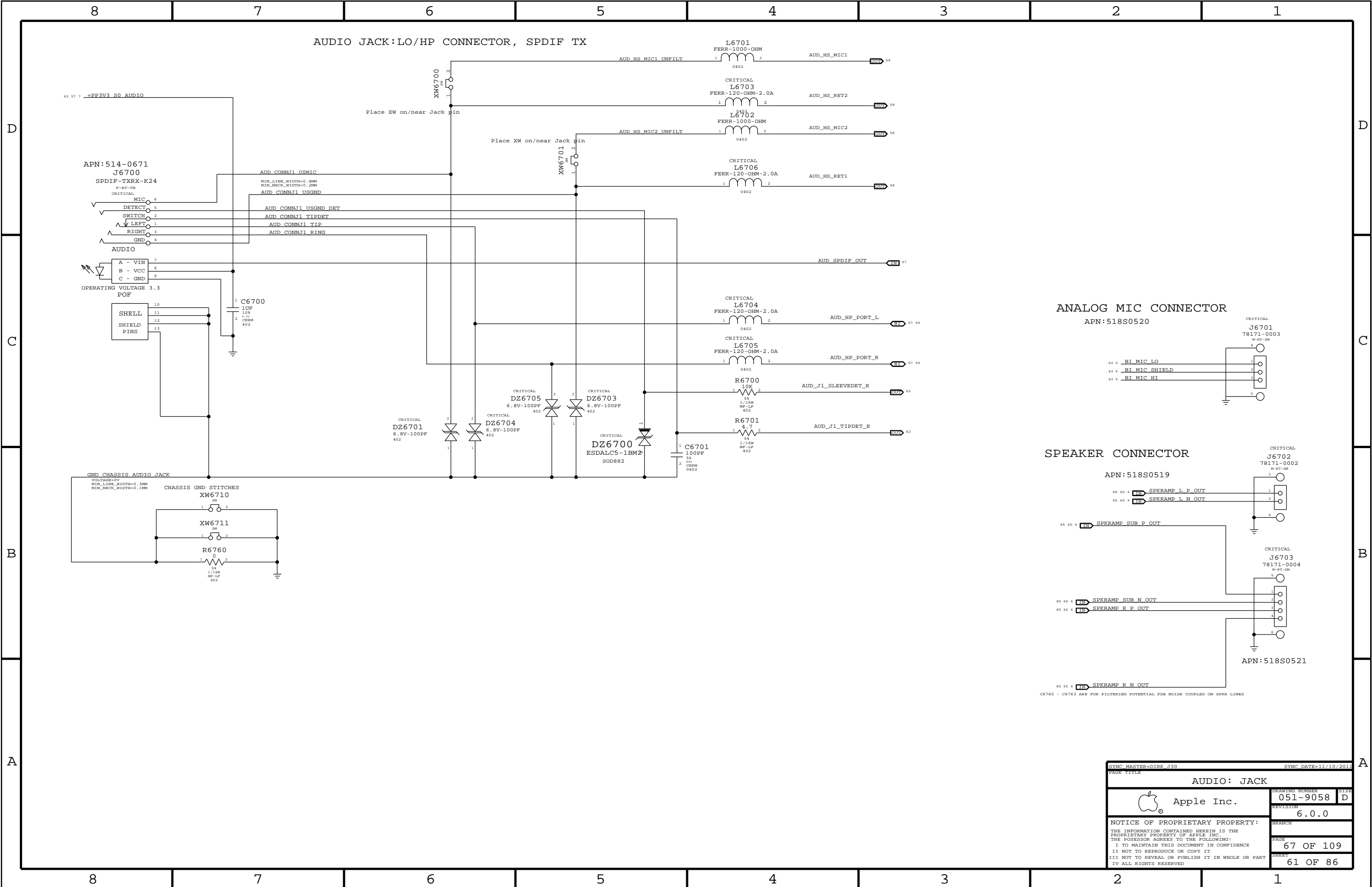



SYNC MASTER=KAVITHA J30		SYNC DATE=07/25/2011	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE D
	REVISION	6.0.0	
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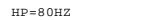
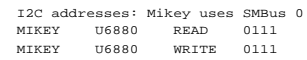
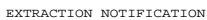



SYNC MASTER=DIRK J3D		SYNC DATE=11/10/2011	
PAGE TITLE			
AUDIO: JACK			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
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		BRANCH	
		PAGE	67 OF 109
		SHEET	61 OF 86

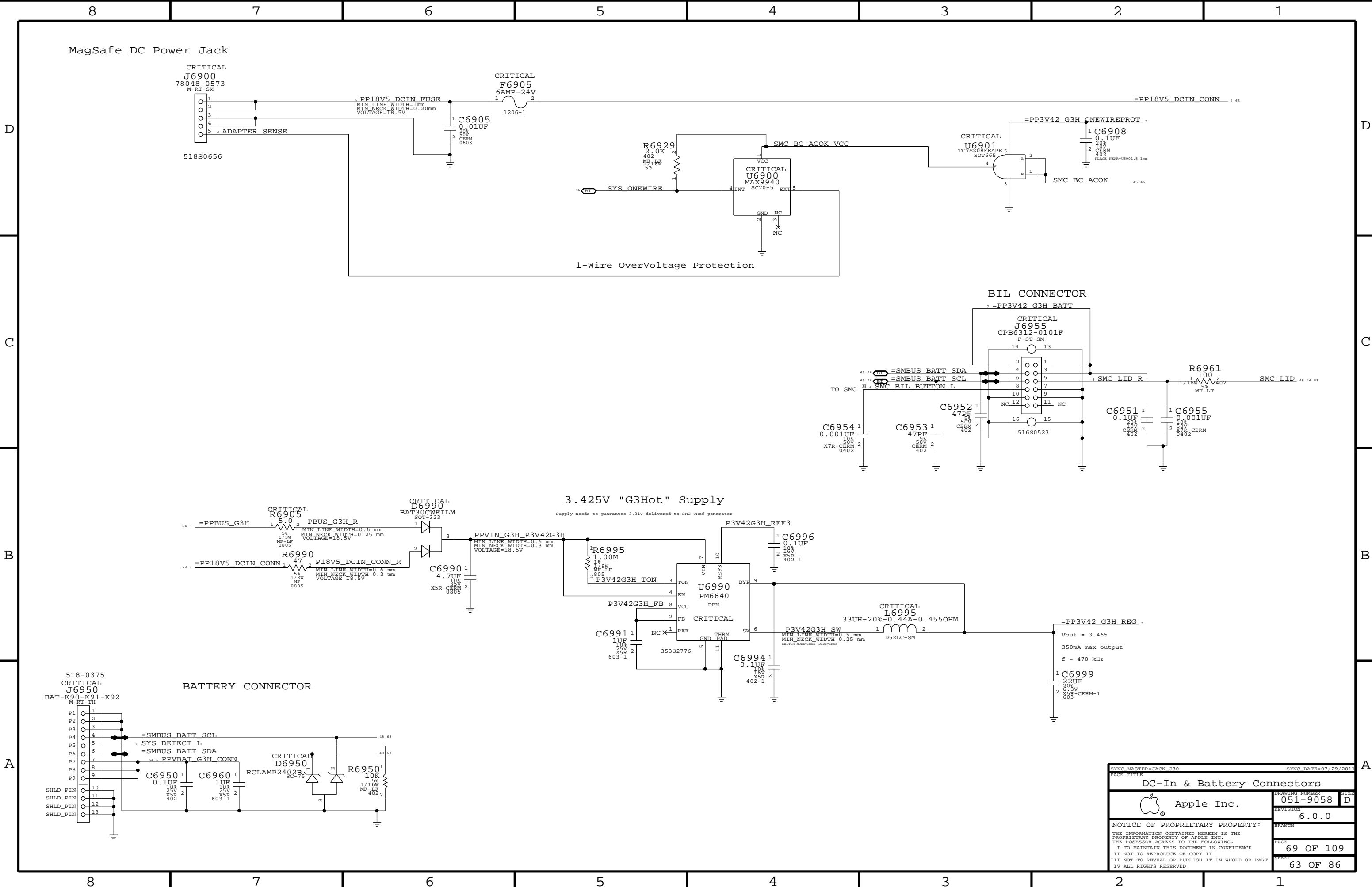
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

FUNCTION	CONVERTER	PIN	COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)		MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)		MIKEY	MIKEY

FUNCTION	FUNCTION	FUNCTION
AUD_IPHS_SWITCH_EN	PANTHER_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	PANTHER_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	PANTHER_POINT GPIO3/PIRQH



SYNCH MASTER=DIRK J30		SYNCH DATE=02/20/2012	
PAGE TITLE		PAGE NO.	
AUDIO:Jack Translators			
		DRAWING NUMBER	SIZE
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		SHEET	62 OF 86




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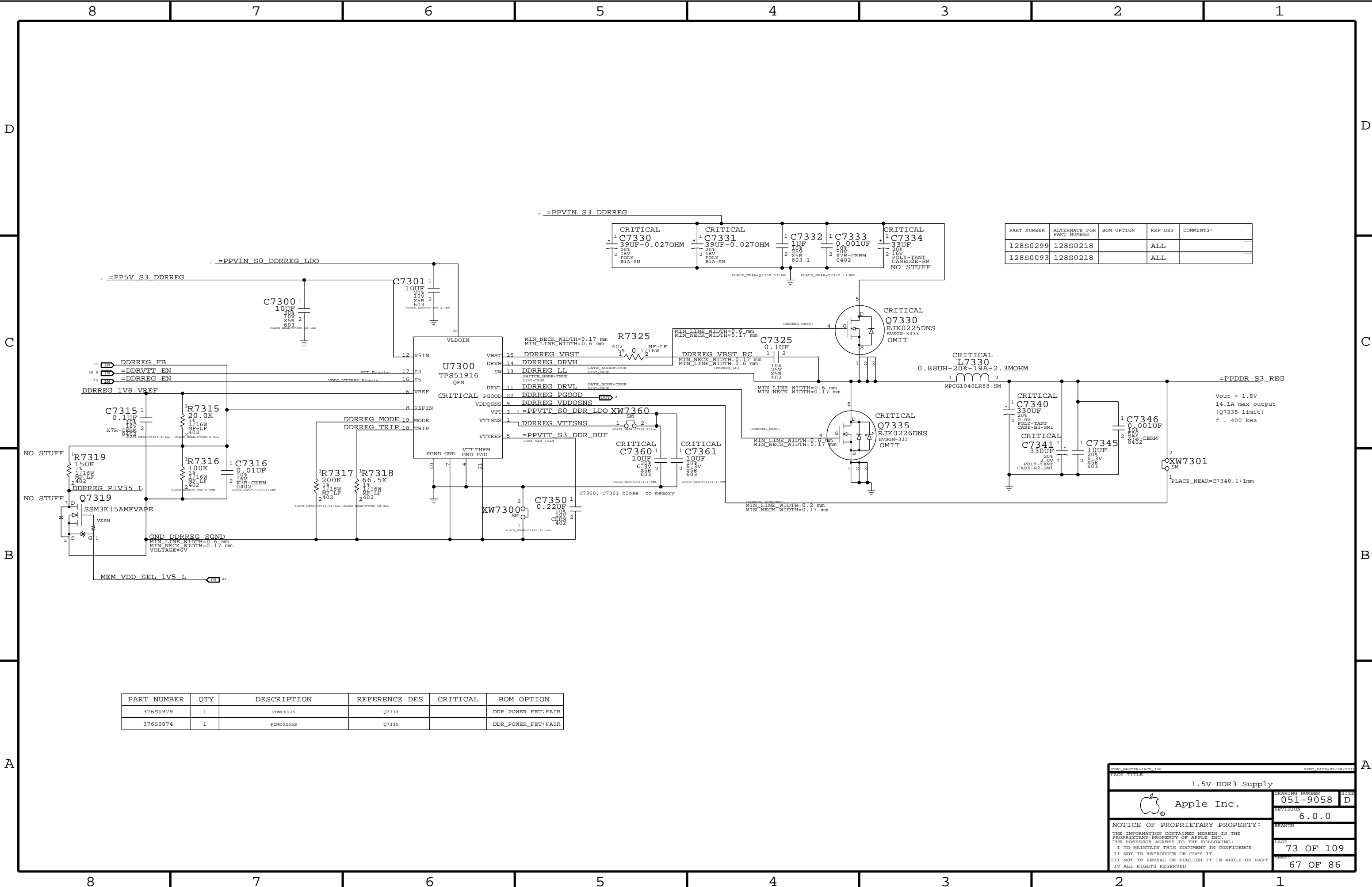
BA1

5V_S3 / 3.3V_S5 POWER SUPPLY

$V_{OUT} = (2 * R_A / R_B) + 2$

$V_{OUT} = (2 * R_C / R_D) + 2$

SYNC MASTER=JACK J30		SYNC DATE=08/22/2013	
PAGE TITLE			
5V/3.3V SUPPLY			
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		BRANCH	
		PAGE	
		72 OF 109	
		SHEET	
		66 OF 86	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0979	1	FDMC0225	Q7330		DDR_POWER_FET:FAIR
376S0874	1	FDMC0202S	Q7335		DDR_POWER_FET:FAIR

SYNCHARTER-JACK-710

SYNCHARTER-JACK-710

1.5V DDR3 Supply

Apple Inc.

051-9058

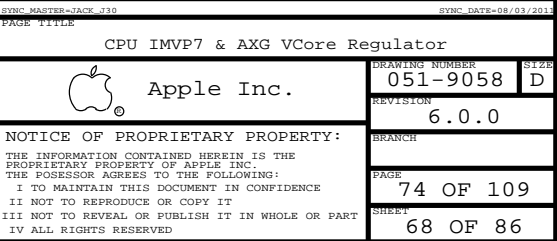
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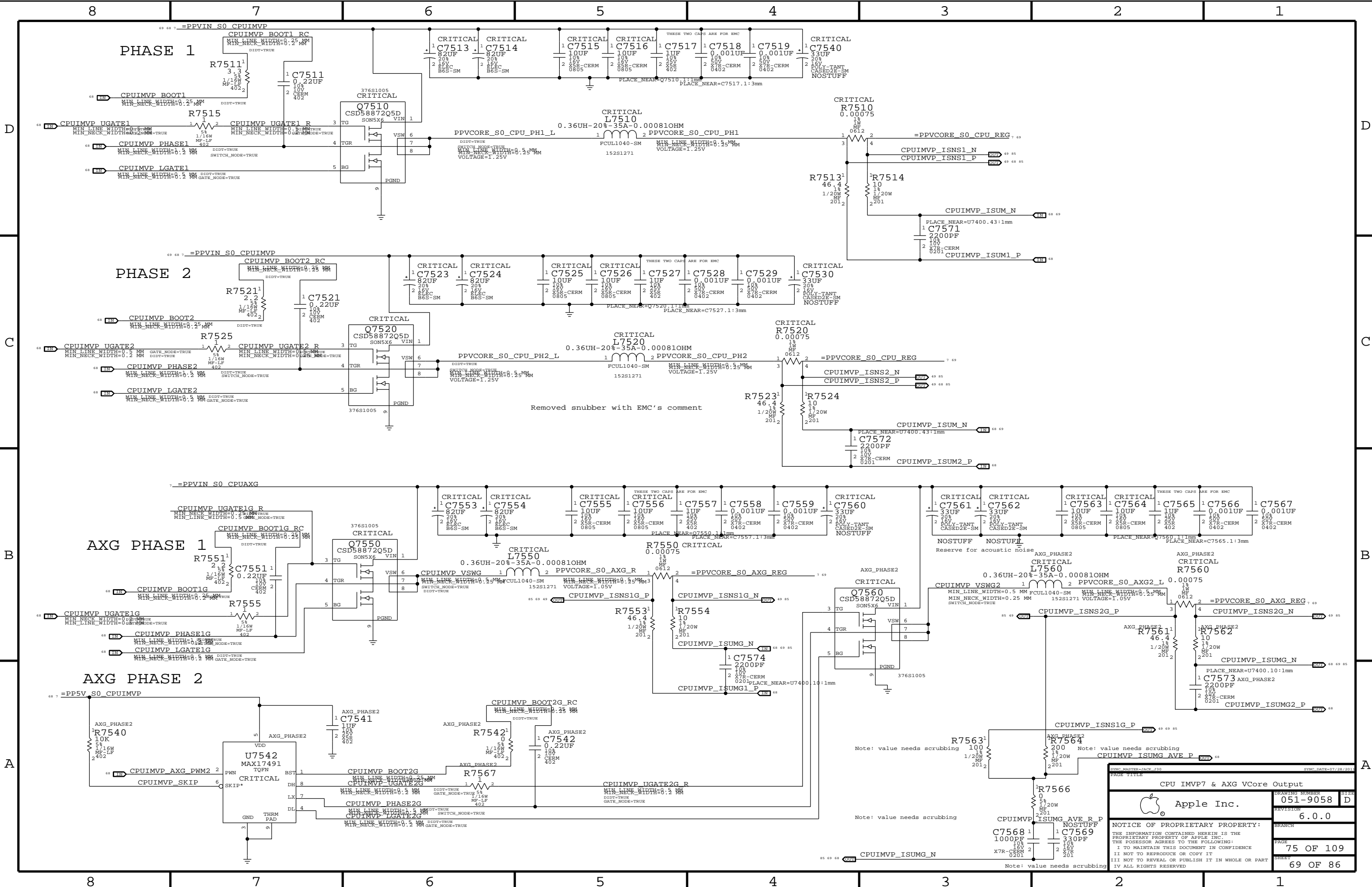
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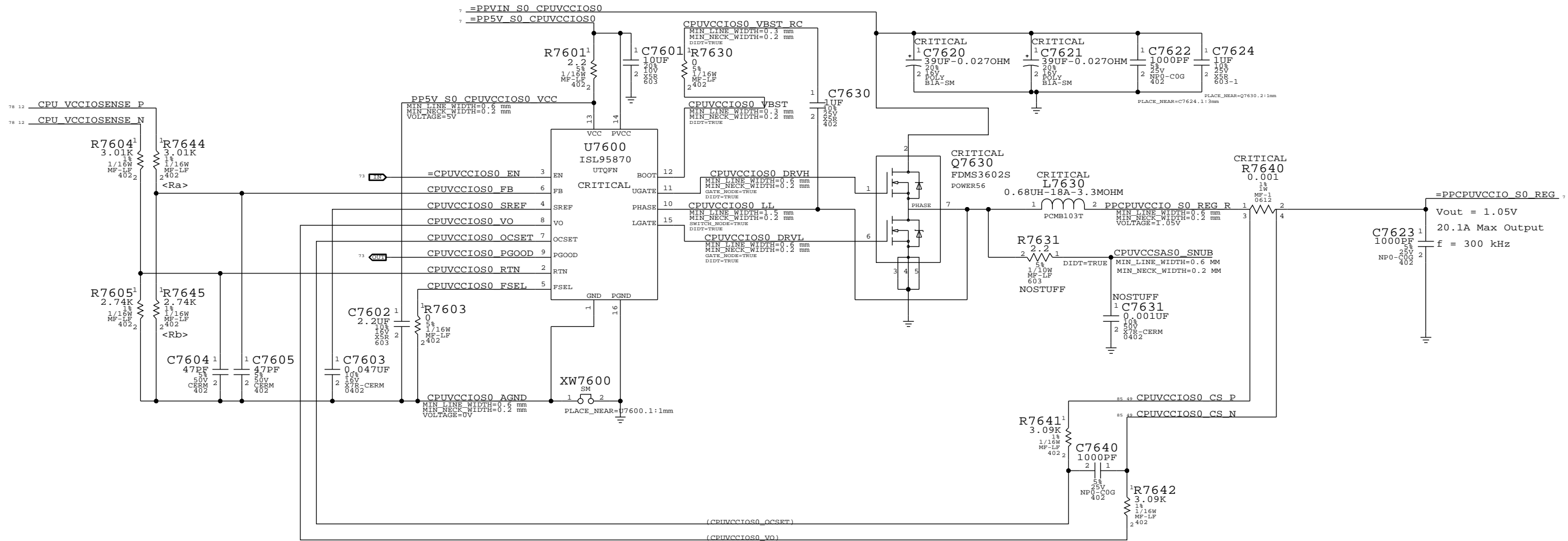
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CPU IMVP7 & AXG VCore Output	
Apple Inc.	DRAWING NUMBER 051-9058
REVISION 6.0.0	SIZE D
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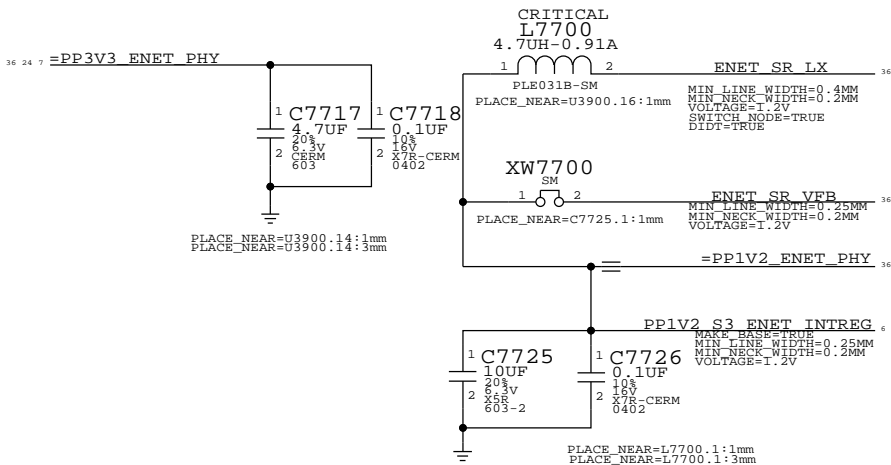
CPU VCCIO (1.05V S0) Regulator



$$OCP = R7641 \times 8.5\mu A / R7640$$
$$OCP = 26.265A$$
$$Vout = 0.5V * (1 + Ra / Rb)$$

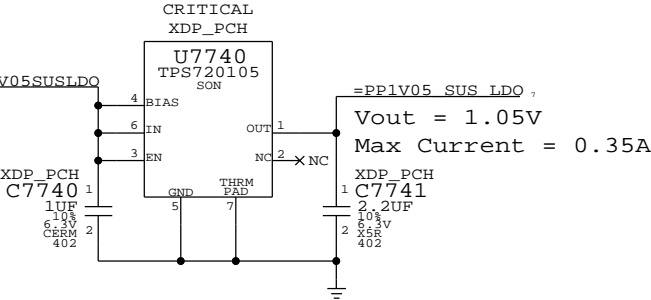
SYNC MASTER=JACK J30		SYNC DATE=09/28/2011	
PAGE TITLE			
CPUVCCIO (1.05V) Power Supply			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE
	REVISION	6.0.0	D
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CAESAR IV 1.2V INT.VR CMPTS

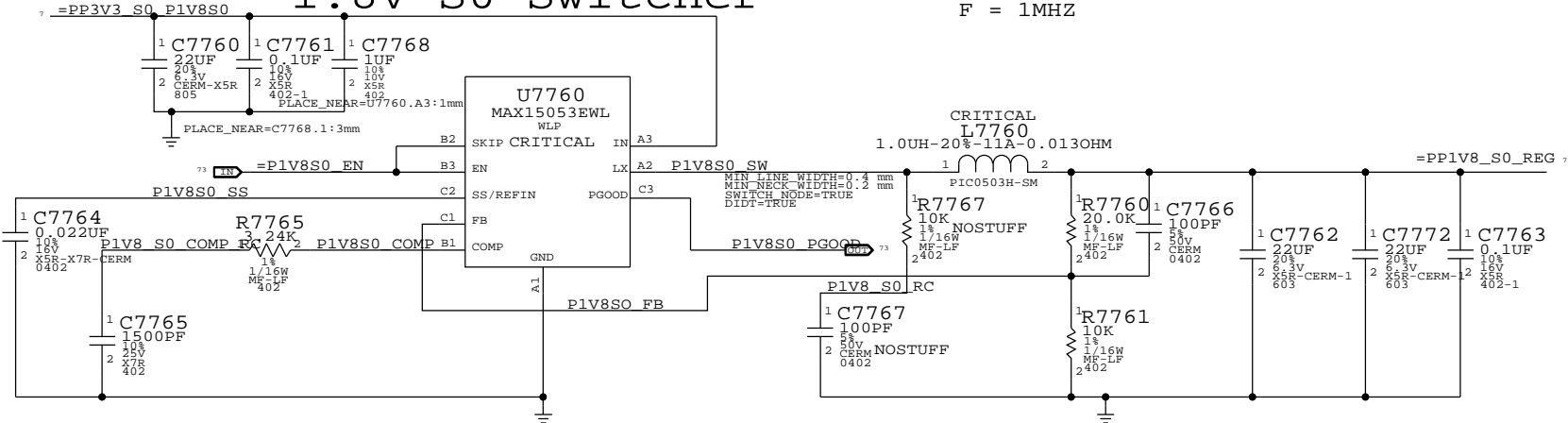


1.05V SUS LDO

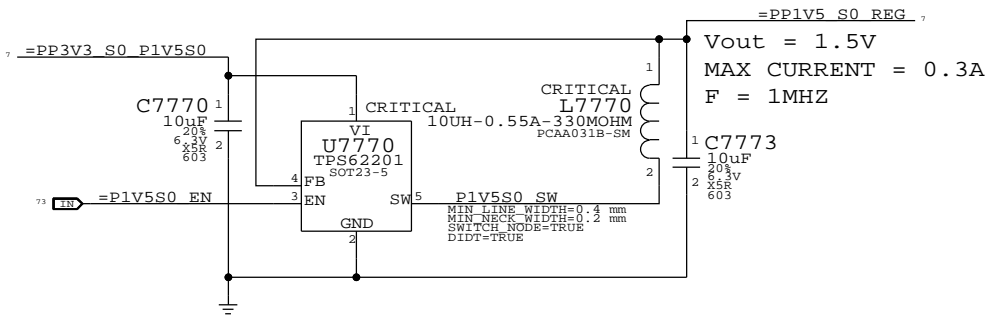
Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



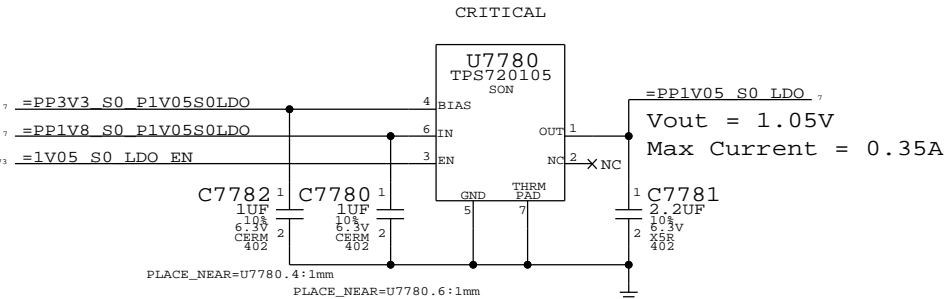
1.8V S0 Switcher




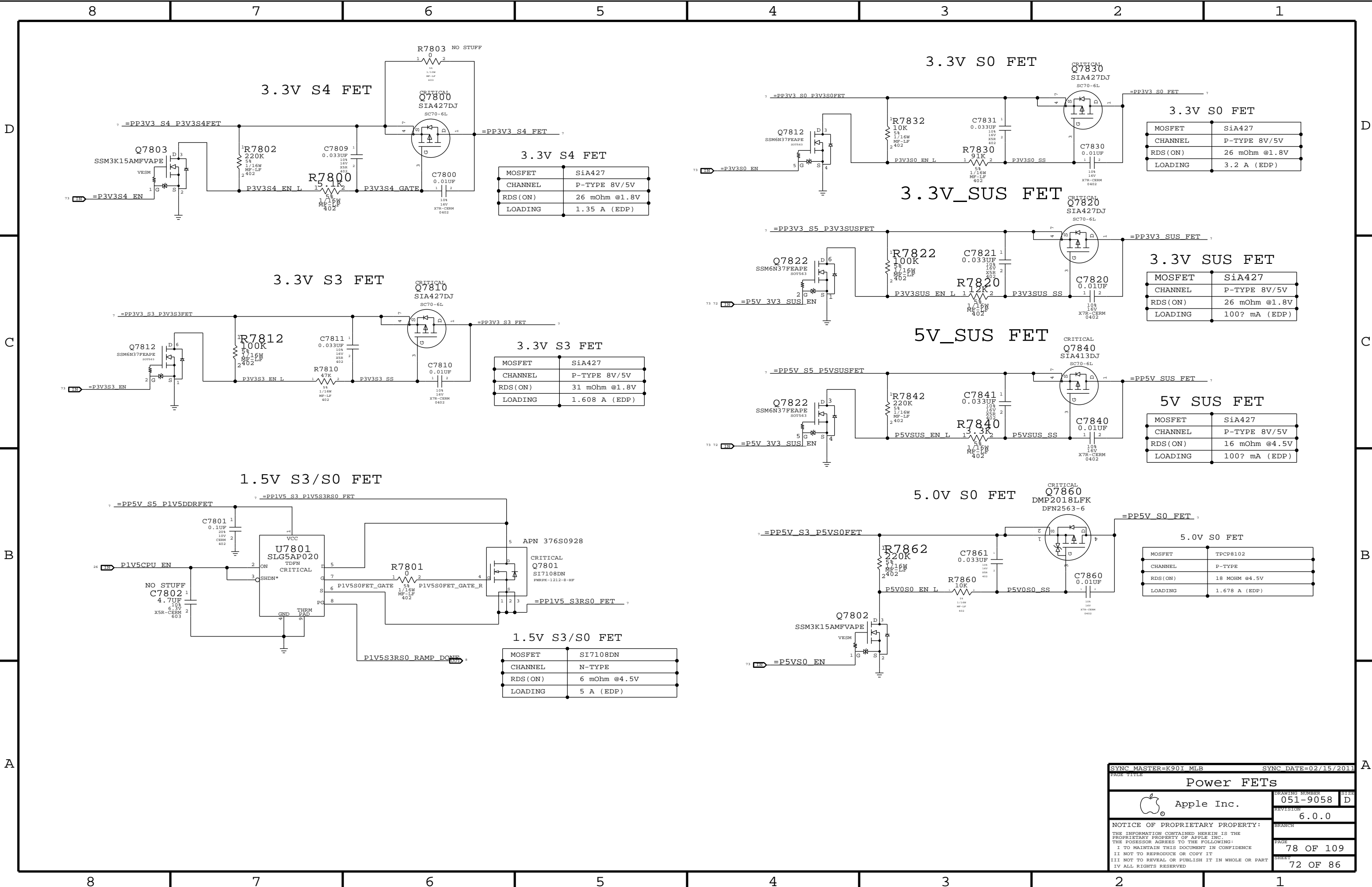
1.5V S0 Switcher

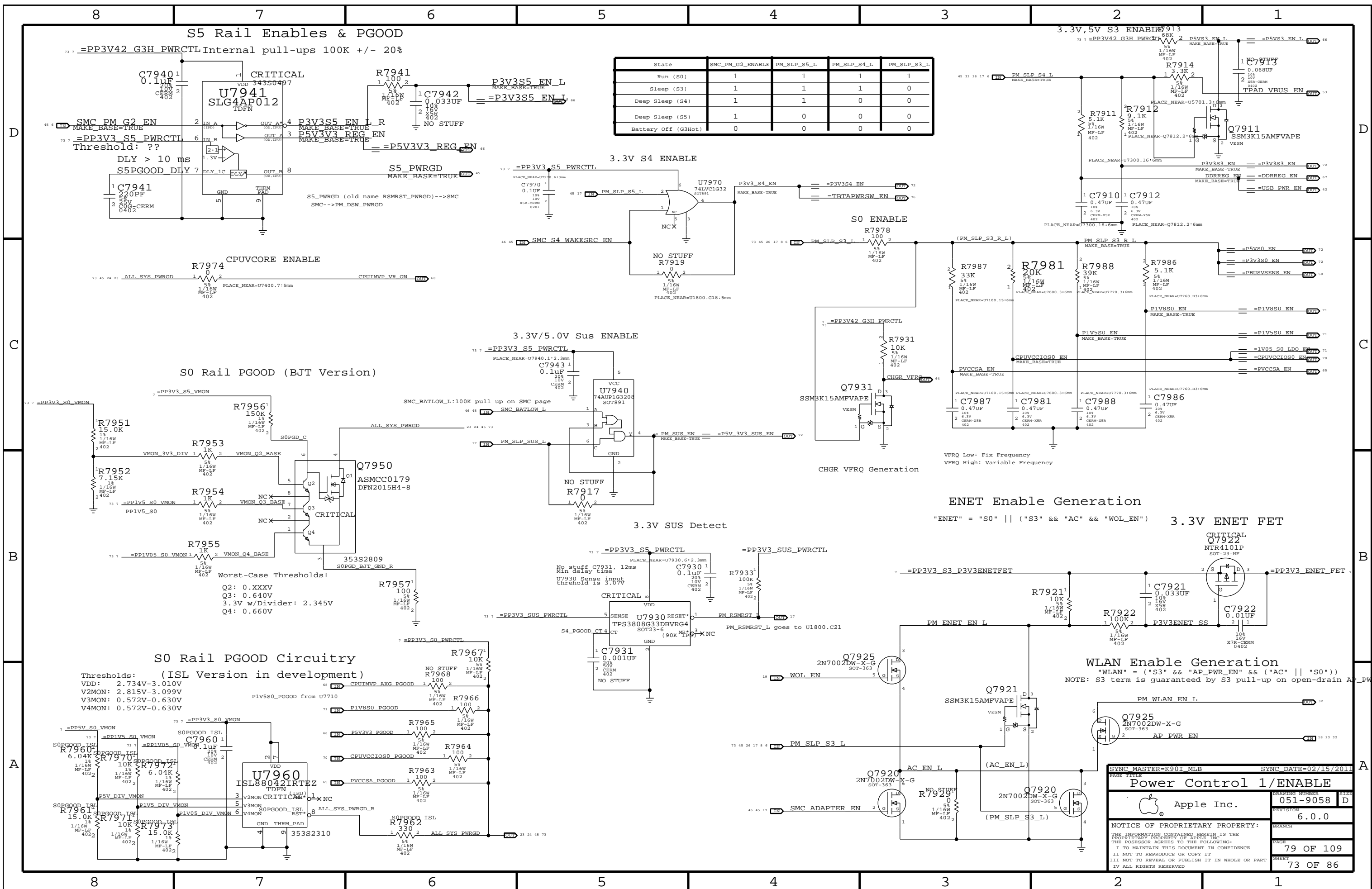


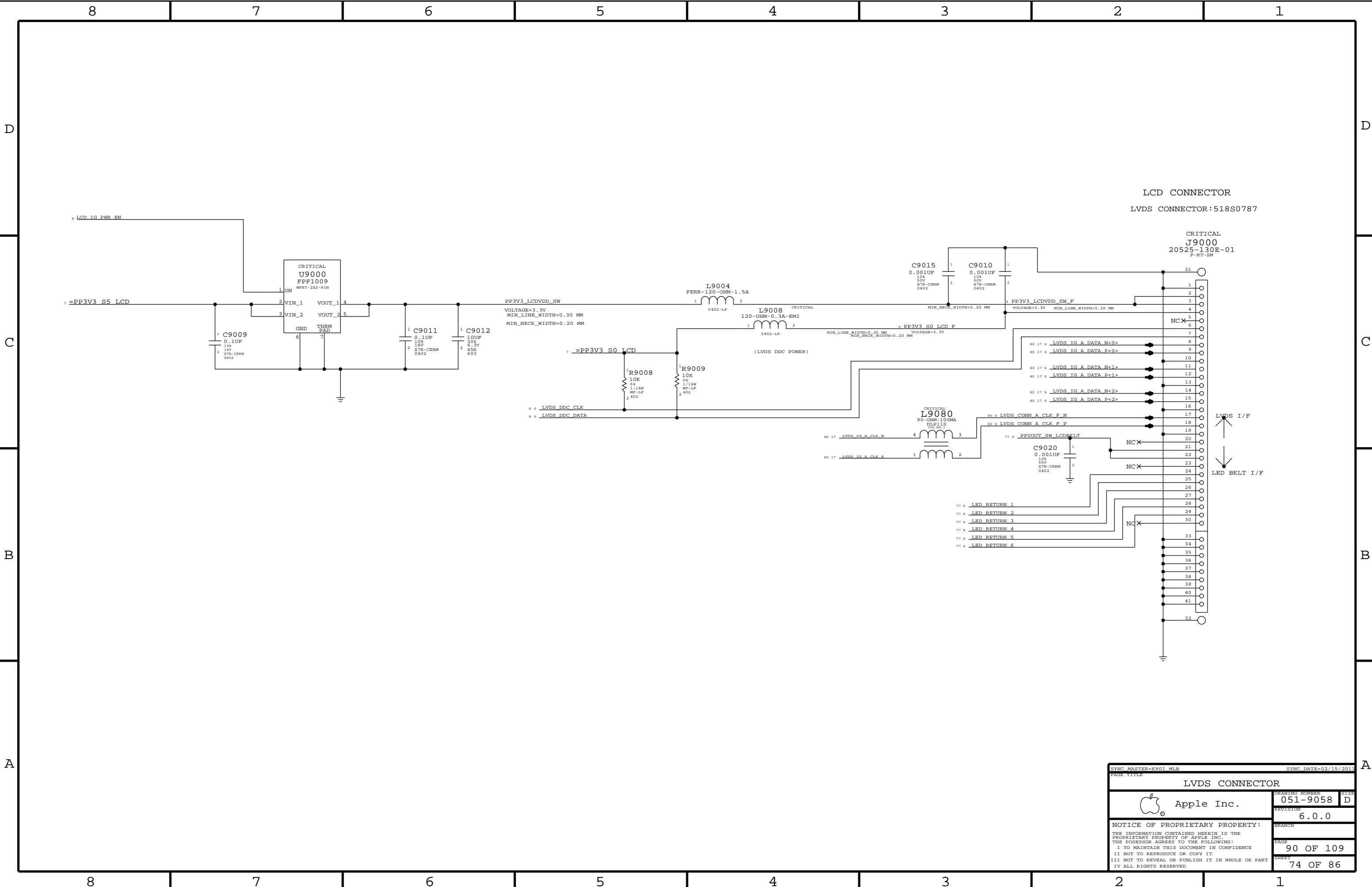
1.05V S0 LDO

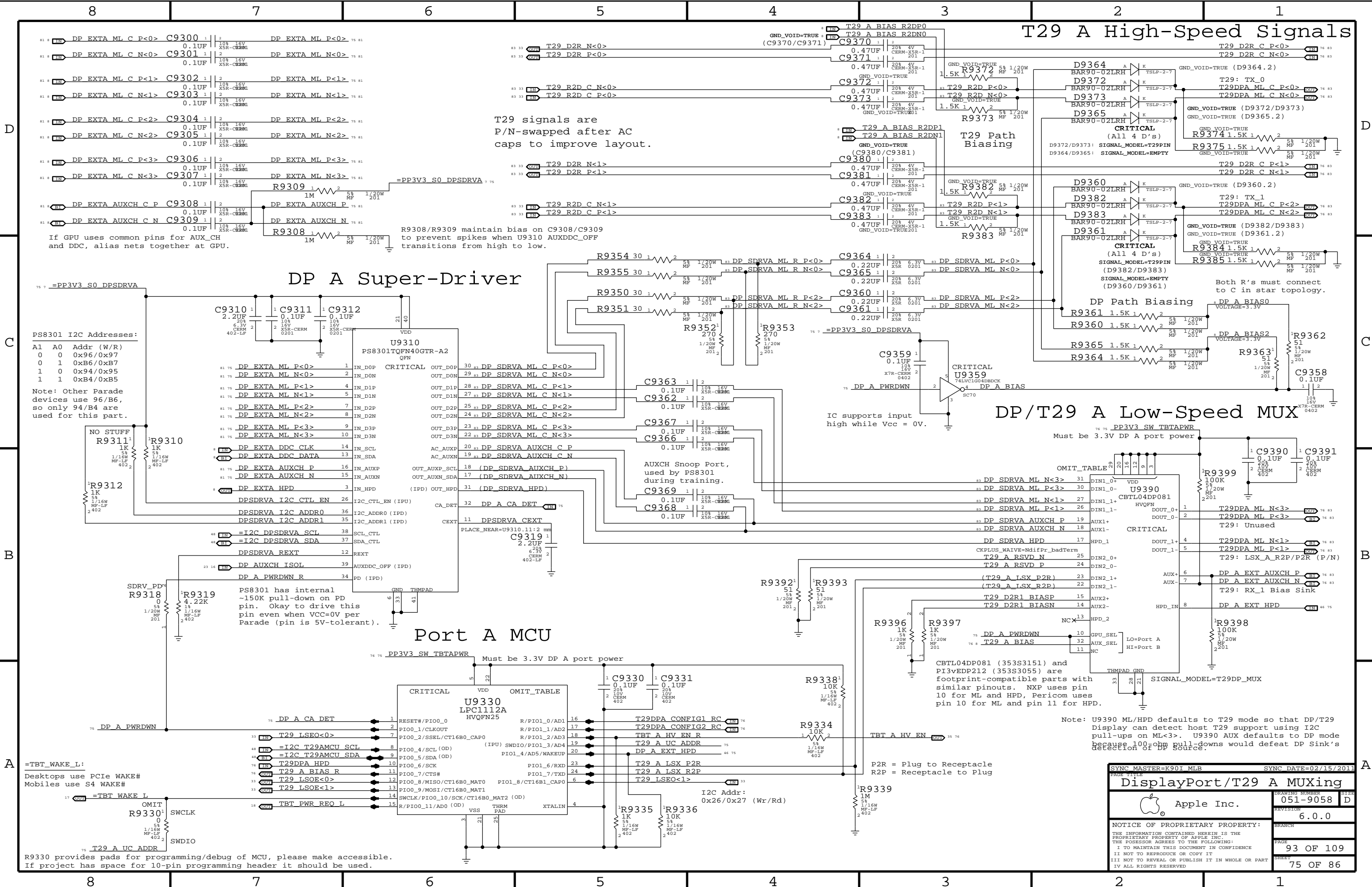


SYNC MASTER=JACK J30		SYNC DATE=07/28/2011	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	051-9058
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T29 A High-Speed Signals

T29 signals are P/N-swapped after AC caps to improve layout.

DP A Super-Driver

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

Port A MCU

DP/T29 A Low-Speed MUX

PAGE TITLE		SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
DisplayPort/T29 A MUXing		DRAWING NUMBER		051-9058	
Apple Inc.		REVISION		6.0.0	
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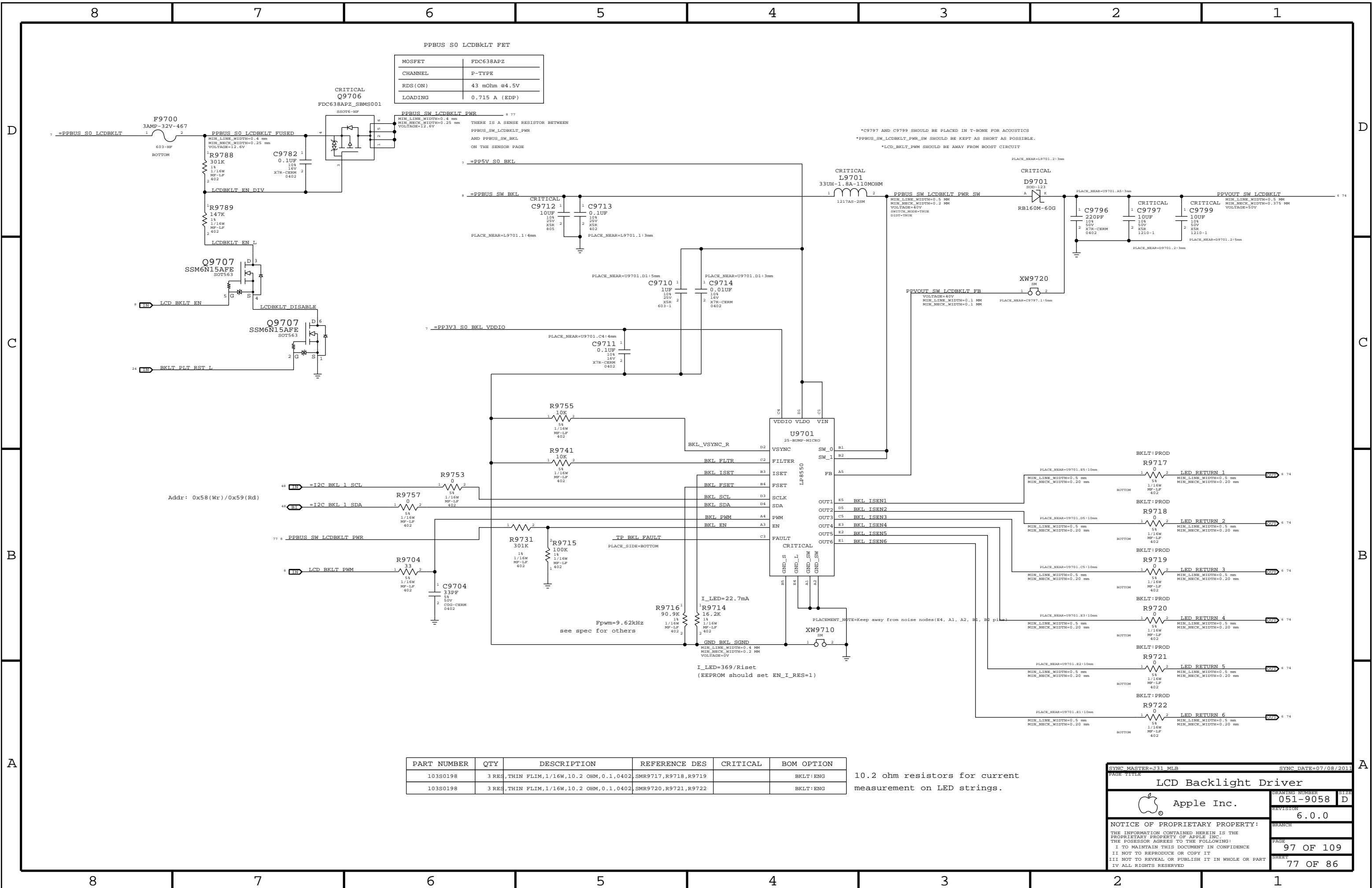
B

D




B

A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3 RES	THIN FLIM,1/16W,10.2 OHM,0.1,0402	SMR9717,R9718,R9719		BKLT:ENG
103S0198	3 RES	THIN FLIM,1/16W,10.2 OHM,0.1,0402	SMR9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=J31 MLB		SYNC DATE=07/08/2011	
PAGE TITLE			
LCD Backlight Driver			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-9058	D
		REVISION	
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCI-Express Signal Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	*	=3X_DIELECTRIC	?
PCIE_T29_TX2RX	*	=4X_DIELECTRIC	?
PCIE_T29_RX2RX	*	=3X_DIELECTRIC	?
PCIE_T29_RX2TX	*	=4X_DIELECTRIC	?
PCIE_T29_2OTHER	*	=3X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	TOP_BOTTOM	=4X_DIELECTRIC	?
PCIE_T29_TX2RX	TOP_BOTTOM	=5X_DIELECTRIC	?
PCIE_T29_RX2RX	TOP_BOTTOM	=4X_DIELECTRIC	?
PCIE_T29_RX2TX	TOP_BOTTOM	=4X_DIELECTRIC	?
PCIE_T29_20THER	TOP_BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_T29_TX	*_TX	*	PCIE_T29_TX2TX
PCIE_T29_TX	*_RX	*	PCIE_T29_TX2RX
PCIE_T29_RX	*_RX	*	PCIE_T29_RX2RX
PCIE_T29_RX	*_TX	*	PCIE_T29_RX2TX
PCIE_T29_TX	*	*	PCIE_T29_2OTHER
PCIE_T29_RX	*	*	PCIE_T29_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LPC_AD	LPC 50S	LPC	LPC AD<3..0>
	LPC_FRAME_L	LPC 50S	LPC	LPC FRAME L
	LPC_RESET_L	LPC 50S	LPC	LPC RESET L
	LPC_CLK33M	CLK LPC 50S	CLK LPC	LPC CLK33M SMC R
	LPC_CLK33M	CLK LPC 50S	CLK LPC	LPC CLK33M SMC
	LPC_CLK33M	CLK LPC 50S	CLK LPC	LPC CLK33M LPCPLUS
	SMBUS_PCH_CLK	SMB 50S	SMB	SMBUS PCH CLK
	SMBUS_PCH_DATA	SMB 50S	SMB	SMBUS PCH DATA
	SMBUS_PCH_0_CLK	SMB 50S	SMB	SMB PCH 0 CLK
	SMBUS_PCH_0_DATA	SMB 50S	SMB	SMB PCH 0 DATA
	SMBUS_SMC_B_00_SCL	SMB 50S	SMB	SMB PCH 1 CLK
	SMBUS_SMC_B_00_SDA	SMB 50S	SMB	SMB PCH 1 DATA
	HDA_RST_CLK	HDA 50S	HDA	HDA BIT CLK
	HDA	HDA 50S	HDA	HDA BIT CLK_R
	HDA_SYNC	HDA 50S	HDA	HDA SYNC
	HDA	HDA 50S	HDA	HDA SYNC_R
	HDA_RST_L	HDA 50S	HDA	HDA_RST_R_L
	HDA	HDA 50S	HDA	HDA_RST_L
	HDA_SDIN0	HDA 50S	HDA	HDA_SDIN0
	HDA	HDA 50S	HDA	AUD_SDI_R
	HDA_SDOOUT	HDA 50S	HDA	HDA_SDOOUT
	HDA	HDA 50S	HDA	HDA_SDOOUT_R
	PM_SUS_CLK	CLK_SLOW	CLK_SLOW	PM_CLK32K_SUSCLK
	SPI_CLK	SPI 50S	SPI	SPI_CLK_R
	SPI	SPI 50S	SPI	SPI_CLK
	SPI_MOSI	SPI 50S	SPI	SPI_MOSI_R
	SPI	SPI 50S	SPI	SPI_MOSI
	SPI_MISO	SPI 50S	SPI	SPI_MISO
	SPI_CS0	SPI 50S	SPI	SPI_CS0_R_L
	SPI	SPI 50S	SPI	SPI_CS0_L
	SPI_MLB_CLK	SPI 50S	SPI	SPI_MLB_CLK
	SPI_MLB_CS_L	SPI 50S	SPI	SPI_MLB_CS_L
	SPI_MLB_MOSI	SPI 50S	SPI	SPI_MLB_MOSI
	SPI_MLB_MISO	SPI 50S	SPI	SPI_MLB_MISO
	SPI_SMC_MISO	SPI 50S	SPI	SPI_SMC_MISO
	SPI_SMC_MOSI	SPI 50S	SPI	SPI_SMC_MOSI
	SPI_SMC_CLK	SPI 50S	SPI	SPI_SMC_CLK
	SPI_SMC_CS_L	SPI 50S	SPI	SPI_SMC_CS_L
	PCIE_ENET_R2D_P	PCIE 85S	PCIE_RCH_TX	PCIE_ENET_R2D_P
	PCIE_ENET_R2D_N	PCIE 85S	PCIE_RCH_TX	PCIE_ENET_R2D_N
	PCIE_ENET_R2D_C_P	PCIE 85S	PCIE_RCH_TX	PCIE_ENET_R2D_C_P
	PCIE_ENET_R2D_C_N	PCIE 85S	PCIE_RCH_TX	PCIE_ENET_R2D_C_N
	PCIE_ENET_D2R_P	PCIE 85S	PCIE_RCH_RX	PCIE_ENET_D2R_P
	PCIE_ENET_D2R_N	PCIE 85S	PCIE_RCH_RX	PCIE_ENET_D2R_N
	PCIE_ENET_D2R_C_P	PCIE 85S	PCIE_RCH_RX	PCIE_ENET_D2R_C_P
	PCIE_ENET_D2R_C_N	PCIE 85S	PCIE_RCH_RX	PCIE_ENET_D2R_C_N
	PCIE_AP_R2D_P	PCIE 85S	PCIE_RCH_TX	PCIE_AP_R2D_P
	PCIE_AP_R2D_N	PCIE 85S	PCIE_RCH_TX	PCIE_AP_R2D_N
	PCIE_AP_R2D_C_P	PCIE 85S	PCIE_RCH_TX	PCIE_AP_R2D_C_P
	PCIE_AP_R2D_C_N	PCIE 85S	PCIE_RCH_TX	PCIE_AP_R2D_C_N
	PCIE_AP_D2R_P	PCIE 85S	PCIE_RCH_RX	PCIE_AP_D2R_P
	PCIE_AP_D2R_N	PCIE 85S	PCIE_RCH_RX	PCIE_AP_D2R_N
	PCIE_FW_R2D_P	PCIE 85S	PCIE_RCH_TX	PCIE_FW_R2D_P
	PCIE_FW_R2D_N	PCIE 85S	PCIE_RCH_TX	PCIE_FW_R2D_N
	PCIE_FW_R2D_C_P	PCIE 85S	PCIE_RCH_TX	PCIE_FW_R2D_C_P
	PCIE_FW_R2D_C_N	PCIE 85S	PCIE_RCH_TX	PCIE_FW_R2D_C_N
	PCIE_FW_D2R_P	PCIE 85S	PCIE_RCH_RX	PCIE_FW_D2R_P
	PCIE_FW_D2R_N	PCIE 85S	PCIE_RCH_RX	PCIE_FW_D2R_N
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	PCIE_FW_D2R_C_N	PCIE 85S	PCIE_RCH_RX	PCIE_FW_D2R_C_N
	PCIE_AP_D2R_PI_P	PCIE 85S	PCIE_RCH_RX	PCIE_AP_D2R_PI_P
	PCIE_AP_D2R_PI_N	PCIE 85S	PCIE_RCH_RX	PCIE_AP_D2R_PI_N
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	PCIE_AP_R2D_PI_N	PCIE 85S	PCIE_RCH_RX	PCIE_AP_R2D_PI_N
	PEG_CLK100M_P	CLK_PCIE_90S	CLK_PCIE	PEG_CLK100M_P
	PEG_CLK100M_N	CLK_PCIE_90S	CLK_PCIE	PEG_CLK100M_N
	PCIE_CLK100M_ENET_P	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_ENET_P
	PCIE_CLK100M_ENET_N	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_ENET_N
	PCIE_CLK100M_AP_P	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_AP_P
	PCIE_CLK100M_AP_N	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_AP_N
	PCIE_CLK100M_FW_P	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_FW_P
	PCIE_CLK100M_FW_N	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_FW_N
	PCIE_CLK100M_EXCARD_P	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_EXCARD_P
	PCIE_CLK100M_EXCARD_N	CLK_PCIE_90S	CLK_PCIE	PCIE_CLK100M_EXCARD_N
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	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<2>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<5>
	PCU_27P4S	PCU_COMP		TP_PCH_VSS_NCTF<7>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<9>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<9>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<11>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<12>
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	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<22>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<25>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<27>
	PCU_27P4S	PCU_COMP		PCH_VSS_NCTF<29>

Chipset Net Properties

ELECTRICAL CONSTRAINT_SET		NET_TYPE				
		PHYSICAL	SPACING			
DP00	DP_EXTA_ML	DP_85D	DP_RCH_TX	DP_EXTA_ML_C P<3..0>	8	75
DP01	DP_EXTA_ML	DP_85D	DP_RCH_TX	DP_EXTA_ML_C N<3..0>	8	75
DP02	DP_EXTA_ML	DP_85D	DP_RCH_TX	DP_EXTA_ML_P<3..0>	8	75
DP03	DP_EXTA_ML	DP_85D	DP_RCH_TX	DP_EXTA_ML_N<3..0>	8	75
DP04	DP_EXTA_AUXCH	DP_85D	DP_RCH	DP_EXTA_AUXCH_C_P	8	75
DP05	DP_EXTA_AUXCH	DP_85D	DP_RCH	DP_EXTA_AUXCH_C_N	8	75
DP06	DP_EXTA_AUXCH	DP_85D	DP_RCH	DP_EXTA_AUXCH_P	8	75
DP07	DP_EXTA_AUXCH	DP_85D	DP_RCH	DP_EXTA_AUXCH_N	8	75
PCIE00	PCIE_T29_R2D	PCIE_85D	PCIE_T29_RV	PCIE_T29_R2D_C P<3..0>	8	33
PCIE01	PCIE_T29_R2D	PCIE_85D	PCIE_T29_RV	PCIE_T29_R2D_C N<3..0>	8	33
PCIE02	PCIE_T29_R2D	PCIE_85D	PCIE_T29_RV	PCIE_T29_R2D P<3..0>	8	33
PCIE03	PCIE_T29_R2D	PCIE_85D	PCIE_T29_RV	PCIE_T29_R2D N<3..0>	8	33
PCIE04	PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R P<3..0>	8	33
PCIE05	PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R N<3..0>	8	33
PCIE06	PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R C P<3..0>	8	33
PCIE07	PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R C N<3..0>	8	33
PCIE08	PCIE_CLK100M_T29	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_T29_P	16	33
PCIE09	PCIE_CLK100M_T29	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_T29_N	16	33

Clock Net Properties

		NET_TTYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
RT30	SYSCLOCK_CLK32K_RTC	CLK_32K_55G	CLK_32K	SYSCLOCK_CLK32K_RTC 16 24
RT50	SYSCLOCK_CLK25M_SB	CLK_25M_55G	CLK_25M	SYSCLOCK_CLK25M_SB 16 24
RT60		CLK_25M_65G	CLK_25M	SYSCLOCK_CLK25M_SB R 16 24
RT70		CLK_25M_55G	CLK_25M	SYSCLOCK_CLK25M_ENET 24 36
RT80		CLK_25M_55G	CLK_25M	SYSCLOCK_CLK25M_ENET R 24 36
RT90		CLK_25M_55G	CLK_25M	SYSCLOCK_CLK25M_T29 24 33
RT95		CLK_25M_55G	CLK_25M	SYSCLOCK_CLK25M_T29 R 24 33

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius’s T29 Routing Notes

T29 IC Net Properties


NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK0 ML C P<3..0> 8 33
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK0 ML C N<3..0> 8 33
DP_T29SNK0_ML	DP_85D	DP_ECH_TX	DP T29SNK0 ML P<3..0> 33
DP_T29SNK0_ML	DP_85D	DP_ECH_TX	DP T29SNK0 ML N<3..0> 33
DP_85D	DP_85D	DP_ECH	DP T29SNK0 AUXCH C P 8 33
DP_85D	DP_85D	DP_ECH	DP T29SNK0 AUXCH C N 8 33
DP_T29SNK0_AUXCH	DP_85D	DP_ECH	DP T29SNK0 AUXCH P 33
DP_T29SNK0_AUXCH	DP_85D	DP_ECH	DP T29SNK0 AUXCH N 33
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK1 ML C P<3..0> 8 33
DP_85D	DP_85D	DP_ECH_TX	DP T29SNK1 ML C N<3..0> 8 33
DP_T29SNK1_ML	DP_85D	DP_ECH_TX	DP T29SNK1 ML P<3..0> 33
DP_T29SNK1_ML	DP_85D	DP_ECH_TX	DP T29SNK1 ML N<3..0> 33
DP_85D	DP_85D	DP_ECH	DP T29SNK1 AUXCH C P 8 33
DP_85D	DP_85D	DP_ECH	DP T29SNK1 AUXCH C N 8 33
DP_T29SNK1_AUXCH	DP_85D	DP_ECH	DP T29SNK1 AUXCH P 33
DP_T29SNK1_AUXCH	DP_85D	DP_ECH	DP T29SNK1 AUXCH N 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SCL 33 48
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SDA 33 48
DP_85D	T29_SPI_CLK	T29_SPI	T29_SPI_CLK 33
DP_85D	T29_SPI_MOSI	T29_SPI	T29_SPI_MOSI 33
DP_85D	T29_SPI_MISO	T29_SPI	T29_SPI_MISO 33
DP_85D	T29_SPI_CS_L	T29_SPI	T29_SPI_CS_L 33
DP_85D	T29DP_80D	T29DP	T29_R2D C P<3..0> 8 33 75
DP_85D	T29DP_80D	T29DP	T29_R2D C N<3..0> 8 33 75
DP_85D	T29DP_100D	T29DP	T29_D2R P<3..0> 8 33 75
DP_85D	T29DP_100D	T29DP	T29_D2R N<3..0> 8 33 75

Only used on hosts supporting T29 video-in

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET		NET TYPE			
		PHYSICAL	SPACING		
800	T29_R2D0	T29DP_80D	T29DP	T29 R2D P<0>	75
801	T29_R2D0	T29DP_80D	T29DP	T29 R2D N<0>	75
802	T29_R2D1	T29DP_80D	T29DP	T29 R2D P<1>	75
803	T29_R2D1	T29DP_80D	T29DP	T29 R2D N<1>	75
804		T29DP_80D	T29DP	T29 R2D C F P<1..0>	
805		T29DP_80D	T29DP	T29 R2D C F N<1..0>	
806	T29_D2R0	T29DP_100D	T29DP	T29 D2R C P<0>	75 76
807	T29_D2R0	T29DP_100D	T29DP	T29 D2R C N<0>	75 76
808	T29_D2R1	T29DP_100D	T29DP	T29 D2R C P<1>	75 76
809	T29_D2R1	T29DP_100D	T29DP	T29 D2R C N<1>	75 76
810		T29DP_100D	T29DP	T29DPA D2R1 AUXCH P	76
811		T29DP_100D	T29DP	T29DPA D2R1 AUXCH N	76
812					
813		T29DP_80D	T29DP	DP SDRVA ML C P<3..0>	75
814		T29DP_80D	T29DP	DP SDRVA ML C N<3..0>	75
815		T29DP_80D	T29DP	DP SDRVA ML R P<3..0>	75
816		T29DP_80D	T29DP	DP SDRVA ML R N<3..0>	75
817	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<2..0:2>	75 83
818	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<2..0:2>	75 83
819	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML P<3..1:2>	
820	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<3..1:2>	
821	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH P	75
822	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH N	75
823		T29DP_80D	T29DP	DP SDRVA AUXCH C P	75
824		T29DP_80D	T29DP	DP SDRVA AUXCH C N	75
825					
826		T29DP_80D	T29DP	T29DPA ML P<3..0>	75 76
827		T29DP_80D	T29DP	T29DPA ML N<3..0>	75 76
828		T29DP_80D	T29DP	T29DPA ML C P<3..0>	75 76
829		T29DP_80D	T29DP	T29DPA ML C N<3..0>	75 76
830		T29DP_80D	T29DP	DP A EXT AUXCH P	75 76
831		T29DP_80D	T29DP	DP A EXT AUXCH N	75 76
832					
833	T29_R2D2	T29DP_80D	T29DP	T29 R2D P<2>	
834	T29_R2D2	T29DP_80D	T29DP	T29 R2D N<2>	
835	T29_R2D3	T29DP_80D	T29DP	T29 R2D P<3>	
836	T29_R2D3	T29DP_80D	T29DP	T29 R2D N<3>	
837		T29DP_80D	T29DP	T29 R2D C F P<3..2>	
838		T29DP_80D	T29DP	T29 R2D C F N<3..2>	
839	T29_D2R2	T29DP_100D	T29DP	T29 D2R C P<2>	
840	T29_D2R2	T29DP_100D	T29DP	T29 D2R C N<2>	
841	T29_D2R3	T29DP_100D	T29DP	T29 D2R C P<3>	
842	T29_D2R3	T29DP_100D	T29DP	T29 D2R C N<3>	
843		T29DP_100D	T29DP	T29DPB D2R3 AUXCH P	
844		T29DP_100D	T29DP	T29DPB D2R3 AUXCH N	
845					
846		T29DP_80D	T29DP	DP SDRVB ML C P<3..0>	
847		T29DP_80D	T29DP	DP SDRVB ML C N<3..0>	
848		T29DP_80D	T29DP	DP SDRVB ML R P<3..0>	
849		T29DP_80D	T29DP	DP SDRVB ML R N<3..0>	
850	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP SDRVB ML P<2..0:2>	83
851	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP SDRVB ML N<2..0:2>	83
852	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP SDRVB ML P<3..1:2>	
853	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP SDRVB ML N<3..1:2>	
854	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH P	
855	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH N	
856		T29DP_80D	T29DP	DP SDRVB AUXCH C P	
857		T29DP_80D	T29DP	DP SDRVB AUXCH C N	
858					
859		T29DP_80D	T29DP	T29DPB ML P<3..0>	
860		T29DP_80D	T29DP	T29DPB ML N<3..0>	
861		T29DP_80D	T29DP	T29DPB ML C P<3..0>	
862		T29DP_80D	T29DP	T29DPB ML C N<3..0>	
863		T29DP_80D	T29DP	DP B EXT AUXCH P	
864		T29DP_80D	T29DP	DP B EXT AUXCH N	

Only used on dual-port hosts.

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PAGE TITLE			
T29 Constraints			
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1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I701_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_I701_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONS	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	-STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P298H
MEM_CND	QND	*	QND_P298H
MEM_CTLG	QND	*	QND_P298H
MEM_DATA	QND	*	QND_P298H
MEM_DQS	QND	*	QND_P298H

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENRT_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCI*	*	GND_P2061
GND	PCI*	*	GND_P2061
GND	SATA*	*	GND_P2061
GND	USB*	*	GND_P2061
SB_POWER	CLK_PCI*	*	PWR_P2061
SB_POWER	SATA*	*	PWR_P2061
SB_POWER	SATA*	*	PWR_P2061

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	LVS*	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4QS OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIB_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIB_90D OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

J30 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACETYPE		
	ENET_100G	ENETCONN	ENETCONN_P<3...0>	37
	ENET_100G	ENETCONN	ENETCONN_N<3...0>	37
	SATA_90D	SATA_RCH_RX	SATA_ODD_D2R_C_P	6 41
	SATA_90D	SATA_RCH_RX	SATA_ODD_D2R_C_N	6 41
	SATA_90D	SATA_RCH_RX	SATA_HDD_D2R_EBROUT_P	41
	SATA_90D	SATA_RCH_RX	SATA_HDD_D2R_EBROUT_N	41
	SATA_90D	SATA_RCH_TX	SATA_HDD_R2D_EBRIN_P	41
	SATA_90D	SATA_RCH_TX	SATA_HDD_R2D_EBRIN_N	41
9393	SATA_90D	SATA_RCH_TX	SATA_HDD_D2R_EBRIN_P	41
9397	SATA_90D	SATA_RCH_TX	SATA_HDD_D2R_EBRIN_N	41
9399	SATA_90D	SATA_RCH_TX	SATA_HDD_R2D_EBROUT_P	41
9399	SATA_90D	SATA_RCH_TX	SATA_HDD_R2D_EBROUT_N	41
	THRM_1200_50G	THRM	THMNS_D1_P	51
	THRM_1200_50G	THRM	THMNS_D1_N	51
9397	THRM_1200_50G	THRM	THMNS_D2_P	51
9399	THRM_1200_50G	THRM	THMNS_D2_N	51
	THRM_1200_50G	THRM	T29_THRMD_P	51
	THRM_1200_50G	THRM	T29_THRMD_N	51
	THRM_1200_50G	THRM	T29THMNS_D3_P	51
	THRM_1200_50G	THRM	T29THMNS_D3_N	51
	ISNS_1200_50G	ISNS	ISNS_HS_COMPUTING_N	50
	ISNS_1200_50G	ISNS	ISNS_HS_COMPUTING_P	50
	ISNS_1200_50G	ISNS	ISNS_HS_OTHER_N	50
	ISNS_1200_50G	ISNS	ISNS_HS_OTHER_P	50
	ISNS_1200_50G	ISNS	CPUVCCIOS0_CS_N	49 70
	ISNS_1200_50G	ISNS	CPUVCCIOS0_CS_P	49 70
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS1_P	49 68
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS1_N	49 69
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS2_P	49 68
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS2_N	49 69
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS1G_P	49 69
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS1G_N	49 69
9399	ISNS_1200_50G	ISNS	CPUIMVP_ISNS2G_P	49 69
9399	ISNS_1200_50G	ISNS	CPUIMVP_ISNS2G_N	49 69
	ISNS_1200_50G	ISNS	CPUIMVP_ISUM_R_P	49
	ISNS_1200_50G	ISNS	CPUIMVP_ISUM_R_N	49
	ISNS_1200_50G	ISNS	CPUIMVP_ISUMG_R_P	49
	ISNS_1200_50G	ISNS	CPUIMVP_ISUMG_R_N	49
9399	ISNS_1200_50G	ISNS	CPUIMVP_ISNSG_P	49
9399	ISNS_1200_50G	ISNS	CPUIMVP_ISNSG_N	49
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS_P	49
	ISNS_1200_50G	ISNS	CPUIMVP_ISNS_N	49
9397	ISNS_1200_50G	ISNS	VOCBAS0_CS_P	65
9399	ISNS_1200_50G	ISNS	VOCBAS0_CS_N	65
9397	ISNS_1200_50G	ISNS	CPUIMVP_ISUMG_P	68 69
9399	ISNS_1200_50G	ISNS	CPUIMVP_ISUMG_N	68 69
9399	ISNS_1200_50G	ISNS	CPU_THRMD_P	8 9
9399	ISNS_1200_50G	ISNS	CPU_THRMD_N	8 9
9399	ISNS_1200_50G	ISNS	ISNS_5V_S0_HDD_P	49
9399	ISNS_1200_50G	ISNS	ISNS_5V_S0_HDD_R_N	49
9399	ISNS_1200_50G	ISNS	ISNS_5V_S0_HDD_R_P	49
9399	ISNS_1200_50G	ISNS	ISNS_LCDBKLT_N	49
9399	ISNS_1200_50G	ISNS	ISNS_LCDBKLT_P	49
9399	ISNS_1200_50G	ISNS	ISNS_LV5_S3_DMR_P	49
9399	ISNS_1200_50G	ISNS	ISNS_LV5_S3_DMR_N	49
9399	ISNS_1200_50G	ISNS	ISNS_LV5_S3_DMR_R_P	49
9399	ISNS_1200_50G	ISNS	ISNS_LV5_S3_DMR_R_N	49
9399	LVDS_80D	LVDS_RCH_TX	LVDS_CONN_A_CLK_P_N	6 74
9399	LVDS_80D	LVDS_RCH_TX	LVDS_CONN_A_CLK_F_P	6 74


J30 Specific Net Properties


[illegible]

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

SYNCH MASTER=K901 MLB		SYNCH DATE=02/15/2013	
PAGE TITLE		PAGE NUMBER	
Project Specific Constraints			
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8		7		6		5		4		3		2		1									
K90i Board-Specific Spacing & Physical Constraints																							
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION									
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		16.2									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
DEFAULT	*	Y	~50_OHM_SR	~50_OHM_SR	10 MM	0 MM	0 MM																
STANDARD	*	Y	~DEFAULT	~DEFAULT	10 MM	~DEFAULT	~DEFAULT																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
50_OHM_SR	TOP, BOTTOM	Y	0.110 MM	0.090 MM																			
50_OHM_SR	*	Y	0.080 MM	0.080 MM	~STANDARD	~STANDARD	~STANDARD																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
40_OHM_SR	TOP, BOTTOM	Y	0.165 MM	0.165 MM																			
40_OHM_SR	ISL10	N	0.126 MM	0.126 MM	~STANDARD	~STANDARD	~STANDARD																
40_OHM_SR	ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	~STANDARD	~STANDARD	~STANDARD																
40_OHM_SR	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
37_OHM_SR	TOP, BOTTOM	Y	0.190 MM	0.1 MM																			
37_OHM_SR	ISL10	N	0.145 MM	0.1 MM	~STANDARD	~STANDARD	~STANDARD																
37_OHM_SR	ISL3, ISL4, ISL9	Y	0.145 MM	0.1 MM	~STANDARD	~STANDARD	~STANDARD																
37_OHM_SR	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
27P4_OHM_SR	TOP, BOTTOM	Y	0.310 MM	0.2 MM																			
27P4_OHM_SR	*	Y	0.235 MM	0.2 MM	~STANDARD	~STANDARD	~STANDARD																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
55_OHM_SR	TOP, BOTTOM	Y	0.090 MM	0.090 MM																			
55_OHM_SR	*	Y	0.070 MM	0.070 MM	~STANDARD	~STANDARD	~STANDARD																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
72_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
72_OHM_DIFF	ISL3, ISL4, ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM																
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM																
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
85_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM																
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM																
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
90_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
90_OHM_DIFF	ISL3, ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM																
90_OHM_DIFF	ISL9, ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM																
90_OHM_DIFF	TOP, BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
100_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
100_OHM_DIFF	ISL3, ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM																
100_OHM_DIFF	ISL9, ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM																
100_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
110_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
110_OHM_DIFF	ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM																
110_OHM_DIFF	ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM																
110_OHM_DIFF	TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM																
NOTE: These are Intel recommended impedances for PEG, unused on K90i.																							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
48_OHM_SR	TOP, BOTTOM	Y	0.165 MM	0.165 MM																			
48_OHM_SR	*	Y	0.090 MM	0.090 MM	~STANDARD	~STANDARD	~STANDARD																
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																
80_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD																
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM																
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM																
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM																
SPACING_RULE_SET								LAYER		LINE-TO-LINE SPACING		WEIGHT		NET_SPACING_TYPE1				NET_SPACING_TYPE2		AREA_TYPE		SPACING_RULE_SET	
DEFAULT								*		0.1 MM		?		*				*		BGA		BGA_P1MM	
STANDARD								*		~DEFAULT		?		MEM_CLK				*		BGA		BGA_P2MM	
BGA_P1MM								*		~DEFAULT		?		CLK_PCIE				*		BGA		BGA_P2MM	
BGA_P2MM								*		~DEFAULT		?		CLK_SLOW				*		BGA		BGA_P2MM	
SPACING_RULE_SET								LAYER		LINE-TO-LINE SPACING		WEIGHT		SPACING_RULE_SET				LAYER		LINE-TO-LINE SPACING		WEIGHT	
1.5:1_SPACING								*		0.15 MM		?		2X_DIELECTRIC				*		0.140 MM		?	
2:1_SPACING								*		0.2 MM		?		3X_DIELECTRIC				*		0.210 MM		?	
2.5:1_SPACING								*		0.25 MM		?		4X_DIELECTRIC				*		0.280 MM		?	
3:1_SPACING								*		0.3 MM		?		5X_DIELECTRIC				*		0.350 MM		?	
4:1_SPACING								*		0.4 MM		?		6X_DIELECTRIC				*		0.420 MM		?	
														7X_DIELECTRIC				*		0.490 MM		?	
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
1:1_DIFFPAIR								*		Y		~STANDARD		~STANDARD		~STANDARD		~STANDARD		0.1 MM		0.1 MM	
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
85_DIFF_BGA								*		~85_OHM_DIFF		~85_OHM_DIFF		~85_OHM_DIFF		~85_OHM_DIFF		~85_OHM_DIFF		~85_OHM_DIFF		~85_OHM_DIFF	
85_DIFF_BGA								ISL3, ISL4		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
85_DIFF_BGA								ISL9, ISL10		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.																							
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
90_DIFF_BGA								*		~90_OHM_DIFF		~90_OHM_DIFF		~90_OHM_DIFF		~90_OHM_DIFF		~90_OHM_DIFF		~90_OHM_DIFF			
90_DIFF_BGA								ISL3, ISL4		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
90_DIFF_BGA								ISL9, ISL10		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.																							
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_DIFF_BGA								*		~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF		~100_OHM_DIFF			
100_DIFF_BGA								ISL3, ISL4		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
100_DIFF_BGA								ISL9, ISL10		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.																							
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_DIFF								*		N		~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
110_DIFF								ISL3, ISL4		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
110_DIFF								ISL9, ISL10		Y		0.075 MM		0.075 MM						0.125 MM		0.125 MM	
110_DIFF								TOP, BOTTOM		Y		0.085 MM		0.085 MM						0.200 MM		0.200 MM	
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.																							
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
48_OHM_SR								TOP, BOTTOM		Y		0.165 MM		0.165 MM									
48_OHM_SR								*		Y		0.090 MM		0.090 MM		~STANDARD		~STANDARD		~STANDARD			
PHYSICAL_RULE_SET								LAYER		ALLOW ROUTE ON LAYER?		MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
80_OHM_DIFF								*		N		~STANDARD		~STANDARD		~STANDARD		~STANDARD		~STANDARD			
80_OHM_DIFF								ISL3, ISL4		Y		0.115 MM		0.115 MM		0.180 MM		0.180 MM		0.180 MM			
80_OHM_DIFF								ISL9, ISL10		Y		0.115 MM		0.115 MM		0.180 MM		0.180 MM		0.180 MM			
80_OHM_DIFF								TOP, BOTTOM		Y		0.140 MM		0.140 MM		0.190 MM		0.190 MM		0.190 MM			
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